SynQor®

MPFC-115-3PH-270-FP
Power Factor Correction
Full-brick

Military Grade
3-Phase Power Factor Correction Module

115 Vrms L-N	45 Hz to 800 Hz	270 Vdc	1.5 kW	100 °C	1.5%	94%
Input Voltage	Input Frequency	Output Voltage	Output Power	Baseplate Temp	THD	Full Load Efficiency

MPFCQor™

The MilCOTS 3-Phase MPFCQor Power Factor Correction module is an essential building block of an AC-DC power supply. Used in conjunction with one of SynQor's matched 3-Phase AC line filters and a limited amount of stabilizing capacitance, this MPFCQor will draw well-balanced and low-distortion sinusoidal currents from each phase of a 3-Phase AC input. It is designed to comply with a wide range of military standards and is manufactured in the United States.

Designed and manufactured in the USA

Operational Features

- Full-brick form factor
- 1.5 kW continuous rating at 100 °C baseplate temperature
- Semi-regulated output: 270 Vdc
- Compatible with Military Standard 60 Hz, 400 Hz & var. freq. systems
- Meets military standards for harmonic content
- Enables systems with repetitive load transients to pass MIL-STD-461 CE101 requirement by offering superior load current rejection
- Minimal inrush current
- Balanced phase currents
- High power factor (0.98 at 400 Hz / 1.5 kW)
- Minimal external output capacitance needed
- Supports full load current during startup ramp
- Additional input filters available to meet full EMI
- N * 1.5 kW power levels when paralleled

Mechanical Features

- Industry standard Full-brick-size
- Size: 2.486" x 4.686" x 0.512" (63.14 x 119.02 x 13.0 mm)
- Weight: 11.3 oz (320 g)

Protection Features

- Output current limit and auto-recovery short circuit protection
- Auto-recovery input under/over-voltage protection
- Auto-recovery output over-voltage protection
- Auto-recovery thermal shutdown

Control Features

- All control pins referenced to separate floating return
- Asynchronous serial data interface
- AC and DC Power Good outputs
- PFC Enable and Battle Short inputs
- 3.3 V always-on standby power output
- Clock synchronization output

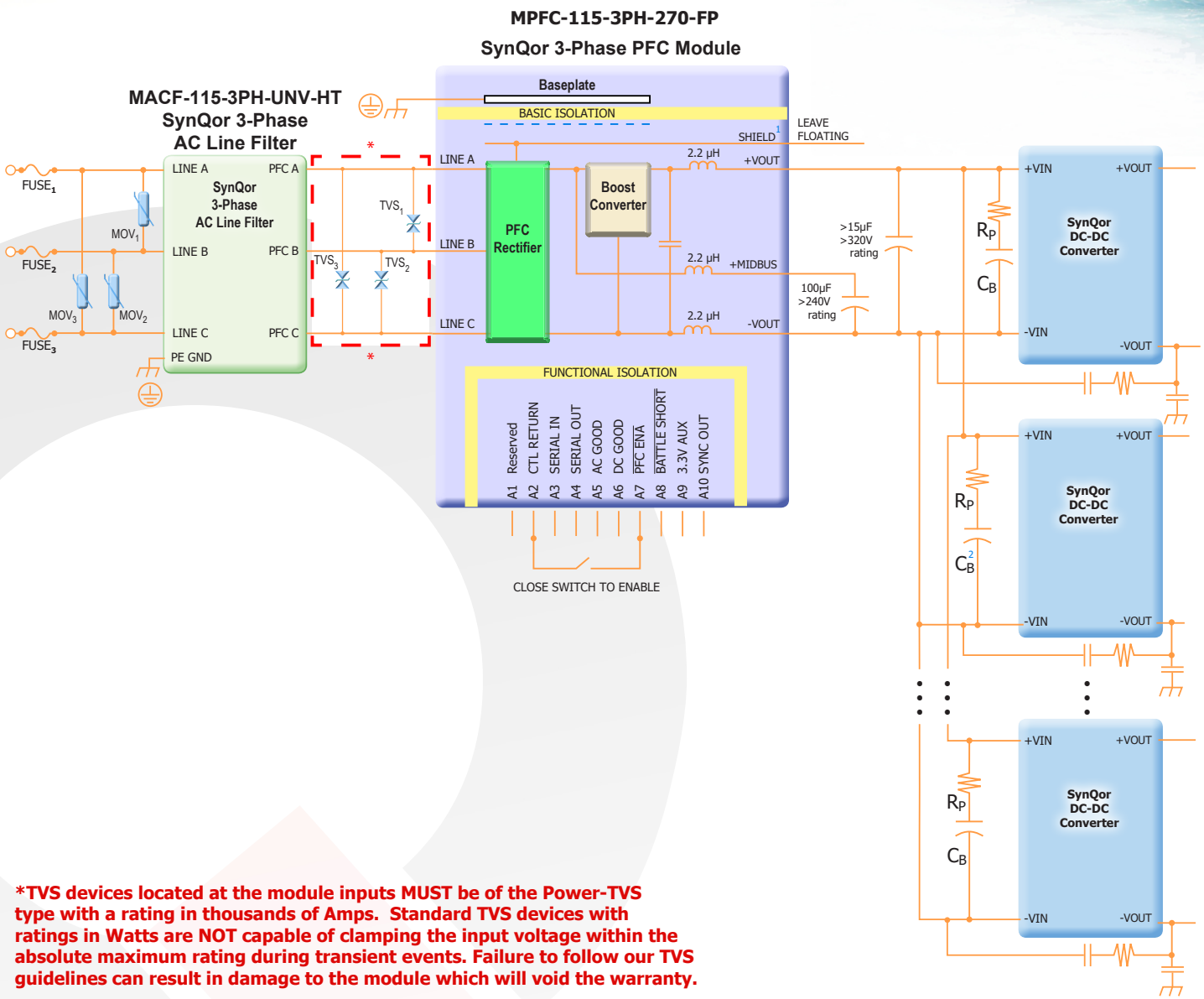
Compliance Features

3-Phase PFCQor series converters are designed to meet:
(With an MCOTS 3-Phase AC input filter)

- MIL-STD-704 (A-F) w/ leading power factor
- MIL-STD-461 (C, D, E, F)
- MIL-STD-1399 (at 200 Vrms L-L)
- MIL-STD-810G

Contents

Typical Application



***TVS devices located at the module inputs MUST be of the Power-TVS type with a rating in thousands of Amps. Standard TVS devices with ratings in Watts are NOT capable of clamping the input voltage within the absolute maximum rating during transient events. Failure to follow our TVS guidelines can result in damage to the module which will void the warranty.**

1 SHIELD pin must be left floating, but may be externally connected to plane under unit near top of PCB to contain high frequency EMI.

2 CB & RP are for stabilizing the system when DC-DC converters are used as the PFC module's load. Additional Hold-Up capacitance may be required for normal operation through interruptions in input power.

3 TVS devices should be selected so that the voltage across the input pins of the MPFC remains below 575 Vpk (L-L) during input spikes or surges.

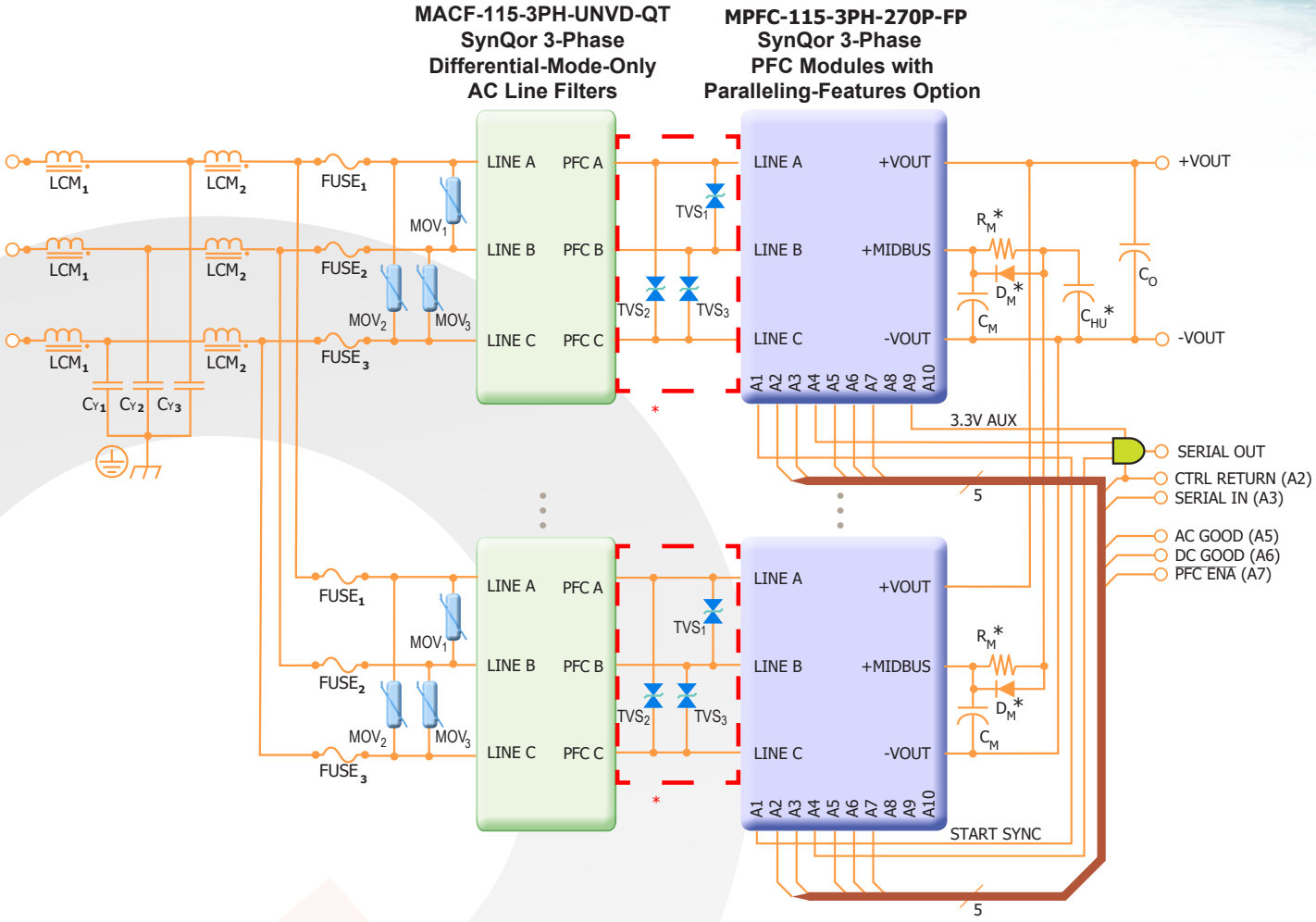
Suggested Parts:

MOV $_{1\text{-}3}$: 300 Vrms, 60 J; EPCOS S10K300E2

TVS $_{1\text{-}3}$: 430 Vpk, 20 J; Littelfuse AK3-430C or Bourns PTVS-430C-TH

Fuse $_{1\text{-}3}$: 250 Vrms, 10 A; Littelfuse 0216010.XEP

Figure A: Typical application of the PFCQor module to create a multiple-output 3-Phase AC-DC power supply



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1 SHIELD pin must be left floating, but may be externally connected to plane under unit near top of PCB to contain high frequency EMI.

2 CB & RP are for stabilizing the system when DC-DC converters are used as the PFC module's load. Additional Hold-Up capacitance may be required for normal operation through interruptions in input power.

3 TVS devices should be selected so that the voltage across the input pins of the MPFC remains below 575 Vpk (L-L) during input spikes or surges.

Suggested Parts:

MOV_{1-3}: 300 Vrms, 60 J; EPCOS S10K300E2

LCM_{1-2}: See Table 1 for recommended construction

$C_{Y\ 1-3}$: 2 x 4.7 nF = 9.6 nF, X7R, 2220, Y2; Murata GA355DR7GF472KW01L

$Fuse_{1-3}$: 250 Vrms, 10 A; Littelfuse 0216010.XEP

TVS_{1-3}: 430 Vpk, 20 J; Littelfuse AK3-430C or Bourns PTVS-430C-TH

R_M*: 4.7 Ω ceramic composition; Ohmite OX47GKE or TE Connectivity CCR14R7KB

D_M*: Fast recovery 8 A; Vishay VS-8EWF04S-M3

*Component optional - used only when C_M value exceeds 1 mF

Figure B: Typical application with multiple PFCQor modules wired in parallel

MPFC-115-3PH-270-FP Electrical Characteristics

Operating Conditions: 115 Vrms L-N (199 Vrms L-L) 3-Phase 400 Hz; 1.5 kW output; baseplate temperature = 25 °C unless otherwise noted. Full operating baseplate temperature range is -55 °C to +100 °C. Specifications subject to change without notice.

Parameter	Min.	Typ.	Max.	Units	Notes & Conditions
ABSOLUTE MAXIMUM RATINGS					
Input Voltage			575	Vpk L-L	Differential across any two line inputs
SERIAL IN and PFC ENA inputs	-2		7	V	Relative to CTL RETURN pin
AC GOOD, DC GOOD, and BATTLE SHORT outputs					
Pull Up Voltage	-2		7	V	Relative to CTL RETURN pin
Sink Current			10	mA	
Operating Temperature	-55		100	°C	Baseplate temperature
Storage Temperature	-65		135	°C	
INPUT CHARACTERISTICS					
Startup Input Voltage Range	85		140	Vrms L-N	147 to 242 Vrms L-L (see note 1)
Operating Input Voltage Range					See section entitled "Power Ratings"
Continuous once started	45		140	Vrms L-N	78 to 242 Vrms L-L
Transient (≤ 1 s)			180	Vrms L-N	312 Vrms L-L
Input Overvoltage Protection (Between any two line inputs)	485	500		Vpk L-L	Threshold levels guaranteed by design
Operating Input Frequency	45		800	Hz	See note 1
Source Inductance			1	mH	Per phase
Recommended Operating Range with Line Imbalance					
Amplitude Imbalance			5	Vrms L-N	
Phase Imbalance			5	deg	
Thresholds for Phase Drop Warning & Shutdown					Warning causes BATTLE SHORT pin to go high
Amplitude Imbalance		37		Vrms L-N	0.25s shutdown delay
Phase Imbalance		18		deg	"
Inrush of AC Input Current			1	A	Output cap is charged later during startup ramp
Power Factor		0.98			400 Hz, 1.5 kW
Reactive Power (per phase)		64		VAR	Zero load (see note 2); Leading
Total Harmonic Distortion of AC Input Current		1.5	2.5	%	Full load (see figure for data vs. load)
Enabled AC Input Power, No Load (sum of phases)					See note 2
400Hz		9.0		W	
60Hz		6.1		W	
Disabled AC Input Power (sum of phases)					See note 2
400Hz		6.0		W	
60Hz		3.1		W	
Maximum Input Current (per phase)			6	Arms	Provided for rating of circuit / fuse
+VOUT OUTPUT CHARACTERISTICS					
+VOUT Steady-State Voltage at Zero Load	272	275	278	V	
+VOUT Controlled Voltage Droop at Full Load	-22	-18	-12	V	See figure "+VOUT voltage vs. load current"
+VOUT Steady-State Voltage Ripple					With minimum +VOUT capacitance and balanced line
Peak-to-Peak (DC to 10 MHz)			1.8	Vpk-pk	
RMS Ripple (DC to 10 MHz)			0.9	Vrms	
Recommended +VOUT Capacitance	15	15	1000	uF	Use R || D for additional cap
Output Over-Voltage Limit Threshold (Full Temp Range)	300	310	320	V	Cycle-by-cycle limit, guaranteed by design
+MIDBUS OUTPUT CHARACTERISTICS					
+MIDBUS Steady-State Voltage Set Point					For main regulated output, see +VOUT section above
Over Load, Temp, and Line Range of 85 - 180 Vrms L-N	145		230	V	See "+MIDBUS Regulation" in application section
Over Load, Temp, and Line Range of 100 - 180 Vrms L-N	170		230	V	
+MIDBUS Steady-State Voltage Ripple					With minimum output capacitance and balanced line
Peak-to-Peak (DC to 10 MHz)			4.4	Vpk-pk	
RMS (DC to 10 MHz)			2.2	Vrms	
+MIDBUS Current Limit Setpoint	9.5	10.0	10.5	A	See graph of available power vs. input line voltage
Recommended +MIDBUS Capacitance	40	100	1000	uF	Use R || D for additional holdup cap
EFFICIENCY					
From AC 3-Phase Input to Main Output					Includes both PFC Rectifier and Boost stages
100% Load (1.5 kW)		94.1		%	400 Hz (0.3% higher at 60 Hz)
50% Load		94.0		%	400 Hz (0.6% higher at 60 Hz)
From AC 3-Phase Input to MIDBUS Output					Power drawn from MIDBUS avoids Boost losses
100% Load (1.5 kW)		95.4		%	400 Hz (0.3% higher at 60 Hz)
50% Load		95.2		%	400 Hz (0.6% higher at 60 Hz)
DYNAMIC CHARACTERISTICS					
Turn-On Transient					
Start-up Inhibit Time		320		ms	From PFC ENA to 10% nominal +VOUT
Turn-On Time		800		ms	From PFC ENA to 100% nominal +VOUT
+VOUT Overshoot			1	%	
Auto-Restart Time		1		s	See "Protection Features" in application section

Note 1: For initial startup, the input voltage and frequency must be within the valid AC GOOD range specified on page 5.
Note 2: External input filter will contribute to this parameter; refer to the appropriate filter datasheet.

MPFC-115-3PH-270-FP Electrical Characteristics (continued)

Operating Conditions: 115 Vrms L-N (199 Vrms L-L) 3-Phase 400 Hz; 1.5 kW output; baseplate temperature = 25 °C unless otherwise noted. Full operating baseplate temperature range is -55 °C to +100 °C. Specifications subject to change without notice.

Parameter	Min.	Typ.	Max.	Units	Notes & Conditions
FEATURE CHARACTERISTICS					
SERIAL IN					
Idle / Stop State Input Voltage	2.4			V	
Zero / Start State Input Voltage			0.8	V	
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
SERIAL OUT					
Idle / Stop State Output Voltage	2.9	3.1		V	4 mA source current
Zero / Start State Output Voltage		0.2	0.4	V	4 mA sink current
AC GOOD (positive logic)					Startup inhibited until AC GOOD output high
Input Voltage Low Threshold	76	80	84	Vrms L-N	AC GOOD low below this threshold
Input Voltage High Threshold	142	150	158	Vrms L-N	AC GOOD low above this threshold
Hysteresis of Input Voltage Thresholds		1		Vrms L-N	Raises low threshold and lowers high threshold
Line Frequency Low Treshold	43	45	47	Hz	AC GOOD low below this threshold
Line Frequency High Threshold	860	900	940	Hz	AC GOOD low above this threshold
Hysteresis of Line Frequency Tresholds		0		Hz	
Low State Output Voltage		0.2	0.4	V	2 mA sink current
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
DC GOOD (positive logic)					DC Power Good output
Rising threshold		240		V	DC GOOD high above this threshold
Falling threshold		140		V	DC GOOD low below this threshold
Low State Output Voltage		0.2	0.4	V	2 mA sink current
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
PFC ENA (negative logic)					PFC enable input (pull low to enable unit)
Off State Input Voltage	2.4			V	
On State Input Voltage			0.8	V	
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
BATTLE SHORT (negative logic)					Battle short input (pull low to disable protection)
Normal State Input Voltage	2.4			V	
Protection-Disabled State Input Voltage			0.8	V	
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
3.3V AUX					3.3 V output always on regardless of PFC ENA state
Output Voltage Range	3.19	3.30	3.43	V	Over line, load, temp, and life
Source Current			100	mA	
SYNC OUT					Synchronization output at switching frequency
High State Output Voltage	2.9	3.1		V	4 mA source current
Low State Output Voltage		0.2	0.4	V	4 mA sink current
Buck & Boost Switching Frequency	190	196.5	203	kHz	Over temp and life; boost synchronized to buck
ISOLATION CHARACTERISTICS					
Isolation Voltage (Any Pin to Baseplate)			2150	V	Basic insulation
Capacitance (Pin 2-9 to Baseplate)		2.2		nF	
Isolation Voltage (Pin 2-9 to CTL RETURN)			1000	V	Functional insulation
Capacitance (Pin 2-9 to CTL RETURN)		1.0		nF	
Isolation Resistance		100		MΩ	
TEMPERATURE LIMITS FOR POWER DERATING CURVES					
Semiconductor Junction Temperature			125	°C	
Board Temperature			125	°C	
Transformer Temperature			125	°C	
Maximum Baseplate Temperature, Tb			100	°C	
Over-Temperature Protection					Measured at surface of internal PCB
Disable Threshold		125		°C	
Warning Threshold		120		°C	Warning causes BATTLE SHORT pin to go high
Enable Threshold		120		°C	
RELIABILITY CHARACTERISTICS					
Calculated MTBF (MIL-217) MIL-HDBK-217F		853		10^3 Hrs.	Ground Benign, Tb = 70 °C
Calculated MTBF (MIL-217) MIL-HDBK-217F		142		10^3 Hrs.	Ground Mobile, Tb = 70 °C

Mil-STD-810G Qualification

Mil-COTS MIL-STD-810G Qualification Testing

MIL-STD-810G Test	Method	Description
Fungus	508.6	Table 508.6-I
Altitude	500.5 - Procedure I	Storage: 70,000 ft / 2 hr duration
	500.5 - Procedure II	Operating: 70,000 ft / 2 hr duration; Ambient Temperature
Rapid Decompression	500.5 - Procedure III	Storage: 8,000 ft to 40,000 ft
Acceleration	513.6 - Procedure II	Operating: 15 g
Salt Fog	509.5	Storage
High Temperature	501.5 - Procedure I	Storage: 135 °C / 3 hrs
	501.5 - Procedure II	Operating: 100 °C / 3 hrs
Low Temperature	502.5 - Procedure I	Storage: -65 °C / 4 hrs
	502.5 - Procedure II	Operating: -55 °C / 3 hrs
Temperature Shock	503.5 - Procedure I - C	Storage: -65 °C to 135 °C; 12 cycles
Rain	506.5 - Procedure I	Wind Blown Rain
Immersion	512.5 - Procedure I	Non-Operating
Humidity	507.5 - Procedure II	Aggravated cycle @ 95% RH (Figure 507.5-7 aggravated temp - humidity cycle, 15 cycles)
Random Vibration	514.6 - Procedure I	10 - 2000 Hz, PSD level of 1.5 g^2/Hz (54.6 g_{rms}), duration = 1 hr/axis
Shock	516.6 - Procedure I	20 g peak, 11 ms, Functional Shock (Operating no load) (saw tooth)
	516.6 - Procedure VI	Bench Handling Shock
Sinusoidal vibration	514.6 - Category 14	Rotary wing aircraft - helicopter, 4 hrs/axis, 20 g (sine sweep from 10 - 500 Hz)
Sand and Dust	510.5 - Procedure I	Blowing Dust
	510.5 - Procedure II	Blowing Sand

Mil-COTS Converter and Filter Screening

Screening	Process Description	S-Grade	M-Grade
Baseplate Operating Temperature		-55 °C to +100 °C	-55 °C to +100 °C
Storage Temperature		-65 °C to +135 °C	-65 °C to +135 °C
Pre-Cap Inspection	IPC-A-610, Class III	•	•
Temperature Cycling	MIL-STD-883F, Method 1010, Condition B, 10 Cycles		•
Burn-In	100 °C Baseplate	12 Hours	96 Hours
Final Electrical Test	100%	25 °C	-55 °C, +25 °C, +100 °C
Final Visual Inspection	MIL-STD-883F, Method 2009	•	•

Power Topology Overview

As seen in Figure A on page 2, this PFC rectifier takes nominal 115 Vrms (L-N) / 199 Vrms (L-L) 3-phase delta AC at its LINE A/B/C inputs, and uses an active-PFC buck converter to create a loosely regulated DC output at the +MIDBUS pin. This is a true 3-phase rectifier topology, as opposed to a composite of three single-phase rectifiers. An additional cascaded boost stage converts +MIDBUS to the main regulated output at the pin +VOUT. Both outputs (+MIDBUS and +VOUT) are referenced to the –VOUT pin and are not isolated from the line inputs.

The term "line-to-neutral (L-N) voltage" is used in this document even though this converter does not utilize a neutral wire. If a neutral wire is present in the application, it should not be connected to the PFC.

Performance

Efficiency and Power Dissipation

Output power may be drawn either from the buck output at +MIDBUS or from the boost output at +VOUT. Drawing power directly from +MIDBUS avoids boost-stage losses and therefore results in higher efficiency. Nonetheless, drawing power from the +VOUT boost output may be desirable even though it incurs an efficiency penalty because +VOUT has better regulation, remaining at its normal output voltage even during line interruptions (provided holdup capacitance is placed at +MIDBUS; see Figure 15 and Figure 17). Efficiency is shown in Figure 1, corresponding power dissipation in Figure 2, and variance over temperature in Figure 3.

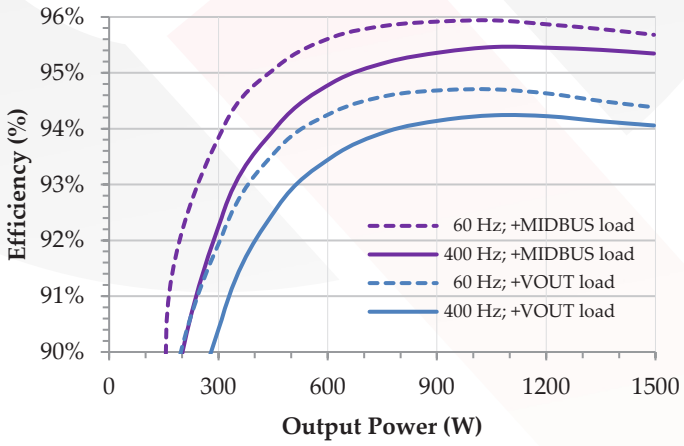


Figure 1: Efficiency vs. output power. Input: 3-phase 115 Vrms (L-N). Baseplate temperature: 30 °C.

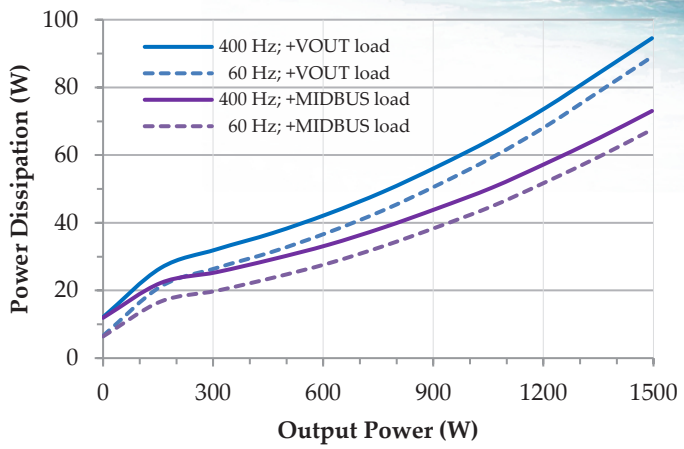


Figure 2: Power dissipation vs. output power. Input: 3-phase 115 Vrms (L-N). Baseplate temperature: 30 °C.

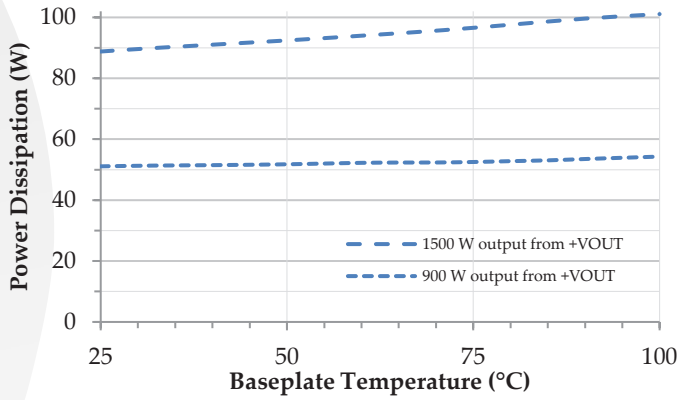


Figure 3: Power dissipation vs. baseplate temperature. Load applied at +VOUT. Input: 60 Hz 3-phase 115 Vrms (L-N).

Input Current Distortion

Legacy diode rectifier solutions typically use bulky magnetics, while having relatively high distortion at line harmonics. In contrast, this modern PFC rectifier switches at high frequency, providing for very low distortion while using small and light internal magnetics. Active current control yields low harmonic content and well-balanced phase currents, even with phase and/or amplitude imbalance on the line inputs.

Input current harmonic content is typically excellent above 25% of full rated output power, increasing somewhat at light loads due to buck converter discontinuous mode operation (see Figure 4). Input current THD will increase with higher input voltage THD. Power may be drawn from either +MIDBUS or +VOUT with similar characteristics.

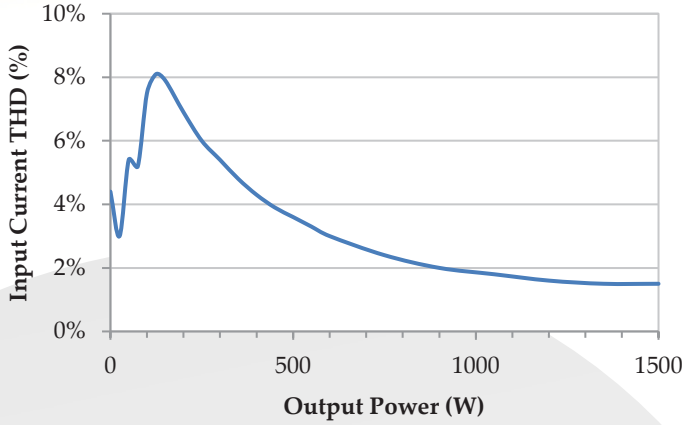


Figure 4: Input Current THD over full load range; input 3-phase 400 Hz 115 Vrms (L-N); includes external input filter module, part number MACF-115-3PH-UNV-HT.

Reactive Power at Fundamental

Line capacitance is necessarily integral to the input EMI filter circuitry, which is divided between internal filtering and the external MACF-115-3PH-UNV-HT input filter module. Total reactive power (including the external input filter module) is approximately 100 VAR per phase when running at 400 Hz. This can be seen directly in Figure 6, where input current is leading input voltage by 20 degrees at half rated load power with a 400 Hz input. At full load and 400 Hz operation, the leading phase angle of input current would be improved to 10 degrees. At 60 Hz, reactive power is almost 7 times lower, so the input current phase lead is commensurately smaller: only 3 degrees at half load and 1.5 degrees at full load. Figure 5 shows leading power factor as a function of output power.

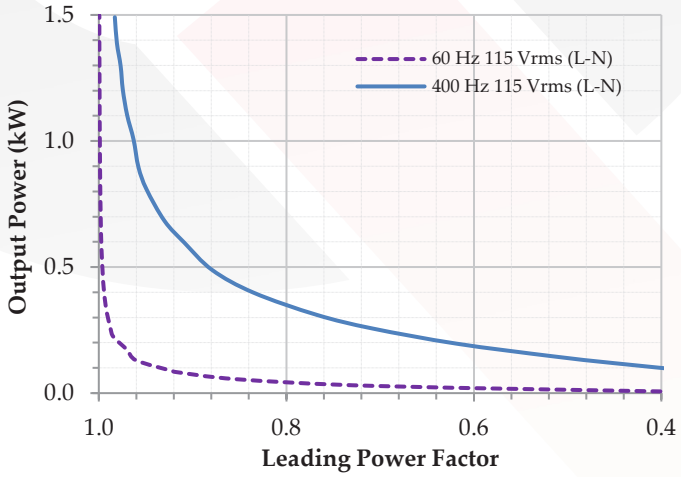


Figure 5: Input leading power factor as a function of operating power level; includes MACF-115-3PH-UNV-HT external input filter module.

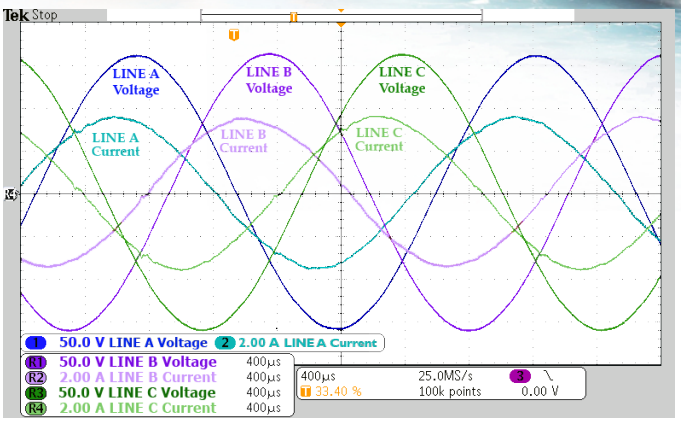


Figure 6: Typical 400 Hz input current waveforms at 50% rated output power; includes MACF-115-3PH-UNV-HT external input filter module.

Power Circuitry Overview

Inrush and Startup

Only a small amount of EMI capacitance resides before the main switches. The PFC buck topology affords excellent control over startup current. Even very large holdup capacitors (at +MIDBUS and/or +VOUT) can be charged gracefully with an actively controlled current limit even with full rated output current applied during the startup ramp (see Figure 7).

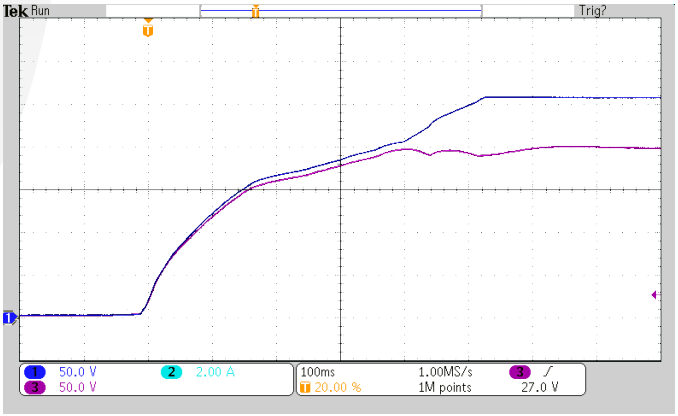


Figure 7: Startup while delivering constant current full rated load: +VOUT (Ch1) and +MIDBUS (Ch3); 1mF at +MIDBUS; 20 µF at +VOUT.

Startup will only proceed after the AC GOOD signal is high. The unit will turn on when all three of the following conditions are met:

1) the $\overline{\text{PFC ENA}}$ pin is pulled low
2) the input voltage is within the valid AC GOOD range (see page 5 for levels and tolerances)
3) the input frequency is within the valid AC GOOD range (see page 5 for levels and tolerances)

Line Transients

The input stage blocks even severe line transients from reaching the output, allowing generous headroom above typical operating input voltage levels.

Line Frequency and Phase Rotation

The PFC does not use an internal phase-locked loop, allowing seamless fast input frequency transients over the full 45 – 800 Hz operating range.

The unit operates equally well with either ABC or CBA input voltage phase rotation.

Common Mode Voltage

The +VOUT and +MIDBUS outputs share a –VOUT return, and all three pins are non-isolated with respect to the 3-phase line inputs. Measured relative to the instantaneous average of all three line inputs (a pseudo-neutral voltage), the –VOUT pin inherently has common-mode ripple voltage at 3x line frequency and approximately 60 Vpk-pk (at nominal line voltage). This is shown in Figure 8, where each signal is measured using a differential probe referenced to the pseudo-neutral line voltage. This ripple is normally not observable, and causes no external current to flow, since in the intended application the AC line is not referred to the DC outputs. Differentially, the voltage from +MIDBUS to –VOUT is DC, with low ripple/noise, as seen in Figure 9. Also note that the +MIDBUS output and –VOUT return are symmetric around the input pseudo-neutral voltage.

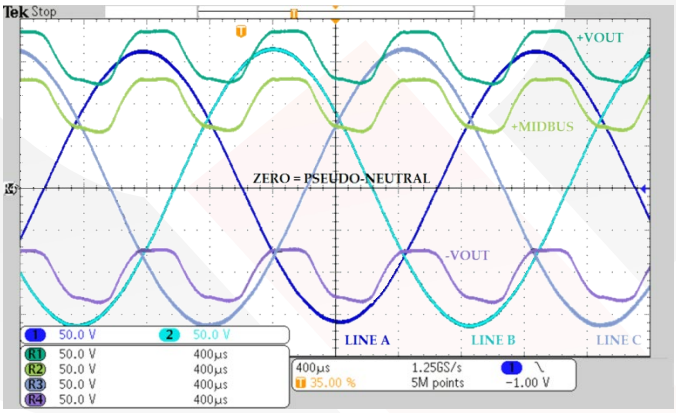


Figure 8: Typical voltages at power pins relative to the instantaneous average of line input voltages: the pseudo-neutral voltage.

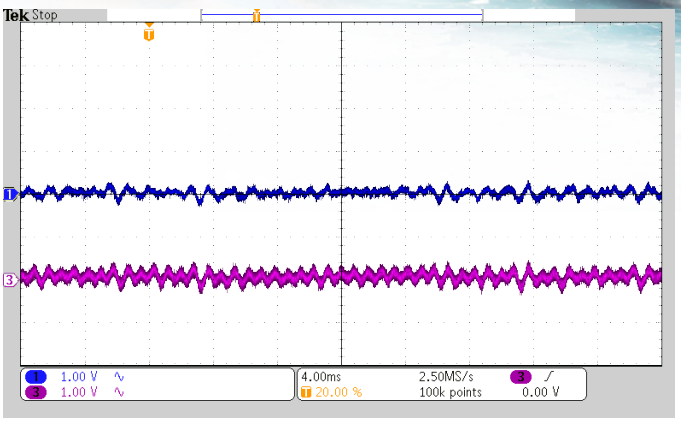


Figure 9: Differential output voltage ripple at +VOUT (Ch1) and +MIDBUS (Ch3); both relative to –VOUT; 400 Hz input; 1.5 kW output power.

+MIDBUS Regulation vs. Line Voltage

Being a buck converter, the main PFC rectifier can only create a +MIDBUS output lower than the instantaneous line-to-line input voltage. The loosely-regulated nominal +MIDBUS output is 200 V at full load. It remains constant at higher input voltages, but is reduced when the AC input is below 100 Vrms (L-N) (see Figure 11).

+VOUT Regulation and Droop

The cascaded boost stage compensates for variations at +MIDBUS. The boost stage is limited to 50% duty cycle, so it is able to maintain nominal +VOUT whenever the +MIDBUS voltage is greater than half the +VOUT voltage.

The main +VOUT output (formed by a cascaded boost converter) is tightly regulated at no-load, but is intentionally allowed to droop down with increased load current (see Figure 10). This droop characteristic fits within the 250 V to 280 V normal voltage range specified for a nominal 270 Vdc bus in MIL-STD-704. It has two important advantages over tight regulation.

First, if the +VOUT output is feeding regulated converters with their constant-power input characteristic, the droop represents additional output resistance which improves input-system stability of these downstream converters.

Second, a droop characteristic improves the worst-case peak deviation of the +VOUT output in response to transient load steps. The peak deviation during a transient is relative to the voltage immediately before the transient: if the nominal output voltage starts lower due to droop at full load, the resulting peak deviation when the load is removed will also be lower.

The boost droop is temperature dependent: the voltage at +VOUT under load will be slightly lower when the unit is hot.

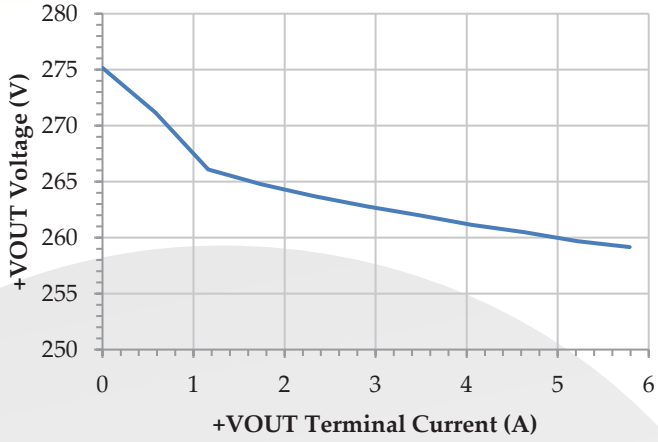


Figure 10: +VOUT voltage vs. load current: a controlled droop characteristic.

PARALLELING GUIDELINES

The available *270P* option (i.e. MPFC-115-3PH-*270P*…) includes several control features to facilitate paralleling. Up to 10 units may be paralleled with outputs directly connected. (More than 10 units may be paralleled when bus converters are used to isolate each PFC output.) A typical application schematic for direct paralleling is shown in Figure B on page 3. Current sharing is achieved via the output voltage droop characteristic shown in Figure 10 above. This sharing method is inherently simple and robust: it is distributed (no master/slave), and involves no communication between units.

Reverse Power Flow

The buck PFC rectifier inherently can only deliver power in the forward direction because each input switch is wired in series with a high voltage diode. The same is true of the boost stage which uses a high voltage diode rectifier. Therefore, current cannot flow backwards from one unit into the output of another unit.

Current Sharing Accuracy

The output voltage is controlled to vary significantly as a computed function of measured current (see Figure 10). The voltage offset and gain is factory calibrated to minimize unit-to-unit variation. This calibration process results in good sharing accuracy: the output power of each unit typically matches the average power to within +/- 50 W. External output wiring resistances should be matched between units for optimum sharing performance.

Features of *270P* Option

Several special features are included in the *270P* model to facilitate paralleling:

1) The START SYNC pin at location A1 is only implemented on the *270P* model. When connected between multiple units, the START SYNC bus actively aligns the restart time between units following an event that causes units to enter hiccup-mode. For instance, when full load is applied, one or more units could experience over-temperature shutdown, causing the remaining units to engage current limit, and 50 ms later entering hiccup due to +MIDBUS under-voltage shutdown. When these units attempt to restart, they may not start because some units are still forced off due to high temperature and the remaining units cannot support full load. When all the units are cool enough to restart, the hiccup times between all units will probably not be aligned, so without START SYNC, the system may still not start. The START SYNC feature delays restart until all units are out of the hiccup state, so that all units will start up simultaneously.
2) The "E" serial port command, only available in the *270P* model, automatically assigns a unique "Net Address" to each unit in the system. All units must be disabled at the time this command is issued. Each unit has a unique 120-bit number stored in ROM, which is encoded onto the START SYNC bus during this enumeration process. The resulting assigned "Net Address" may be used with a shared serial port to communicate individually to each unit in a paralleled system. The "Net Address" reverts to the default value of 'm' when power is cycled, so the enumeration command should be part of the system boot sequence.
3) The "N" serial port command optionally overrides the state of the $\overline{\text{PFC ENA}}$ input, allowing a unit to be forced on or off.
4) The Battle-Short function may be set via the serial port using the "n" command.

Control Connections for Paralleling

The following control signal wiring recommendations for a parallel system are captured in the typical application diagram in Figure B on page 3:

1) The CTL RETURN pins from multiple units should be connected together to provide a common control ground.
2) SERIAL IN and $\overline{\text{PFC ENA}}$ input pins may be wired in parallel.
3) AC GOOD and DC GOOD output pins may be wired in parallel.

4) START SYNC should be connected in parallel between all units in the system (for available *270P* option).
5) The 3.3V AUX outputs could also be paralleled, but total current drawn from 3.3VAUX should not exceed the 100 mA rating of a single unit.
6) SYNC OUT pins should not be connected between units: doing so would cause a logic output contention.
7) The SERIAL OUT signals may be combined using an external AND gate. Alternatively, a multi-drop bus may be formed by pulling the bus low when SERIAL OUT is low, and releasing the bus when SERIAL OUT is high, returning the bus to the idle state via a pull-up resistor. The time constant of this pull-up resistor along with any parasitic capacitance must be much shorter than the baud rate.
8) $\overline{\text{BATTLE SHORT}}$ pins should not be interconnected between units. When not warning of an impending shutdown, the $\overline{\text{BATTLE SHORT}}$ pin is normally pulled low, and this could erroneously cause other units to enter the Battle-Short state. If the $\overline{\text{BATTLE SHORT}}$ protection-warning output function is used in a paralleled system, then individual signals should be combined using an OR gate. If the $\overline{\text{BATTLE SHORT}}$ protection-disable input function is used in a paralleled system, then either a separate pull-down transistor should be used for each unit, or the Battle-Short function may be accessed via the serial port. If a $\overline{\text{BATTLE SHORT}}$ pin is not used, it may be left open.

Power Connections for Paralleling

The following power wiring recommendations for a parallel system are captured in the typical application diagram in Figure B on page 3:

1) +VOUT and –VOUT may be wired directly in parallel.
2) The LINE A/B/C inputs should be wired in parallel upstream of the input filters. Each PFC unit should have its own TVS bank located near the input pins. The input voltage across the MPFC input pins should remain below the maximum rated value of 575 Vpk (L-L)
3) +MIDBUS should *not* be connected directly in parallel between units. It is acceptable to share a single +MIDBUS holdup capacitor between multiple units by connecting multiple R||D elements (from Figure 18) with the configuration shown in Figure B on page 3. The recommended value of +MIDBUS capacitance should be placed locally at each unit.

Input Filter Design for Paralleling

Two different 3-phase AC input filter modules types are available: a half-brick for most applications and a quarter-brick used for direct paralleling applications. The half-brick MACF-115-3PH-UNV-HT integrates both common-mode (CM) and differential-mode (DM) filtering into one module. The half-brick filter may be paired either with a single PFC unit, or may also be used in paralleled applications where the outputs of each PFC unit are individually isolated. When paralleling multiple PFC units with the outputs directly connected, multiple parallel CM input filters cannot be used, because the net current through each will not balance to zero. This would cause the CM cores to saturate and ruin the CM filter performance. Instead, in direct parallel applications, quarter-brick MACF-115-3P-UNVD-QT filter modules are recommended, which implement only differential-mode (DM) filtering. As shown in Figure B on page 3, these DM-only filters are used in conjunction with a single upstream external CM input filter. Since there is only one return path, the net current through the single CM stage is guaranteed to be zero.

Careful design of the common-mode (CM) choke component is critical because any parasitic external magnetically induced current is coupled directly upstream to the input power cable. Winding the choke "trifilar" (with each three-wire bundle of LINE A/B/C wound as a unit) is essential for good CM filtering performance. The quiet end of each winding should not overlap the noisier end: when multiple parallel winding layers are used to reduce resistive losses, each layer should have the full number of turns. Insulation must be rated for the line voltage: PTFE stranded wire conforming to MIL-W-16878/4 is recommended. Low-profile nanocrystalline cores similar to the Nanoperm® LC M-6xx series by Magnetec GmbH are appropriate because the large inner diameter allows for ample winding area. Table 1 presents the recommended construction for each of these external CM chokes. This information is provided as a design starting point for reference only and does not in itself guarantee compliance to any EMI specification.

# of Paralleled PFC Modules	Magnetec LC Core Part #	# of Turns	# of Layers in ||	Wire Gauge	DCR per phase (mΩ @ 25°C)	Wound Thickness (mm)	Wound Diameter (mm)
2	M-607	7	1	20	7.0	11	27
3	M-608	9	2	20	5.1	14	35
4-5	M-610	13	2	16	4.4	17	52
6	M-633	16	3	16	4.2	21	66
7-8	M-634	18	3	14	3.3	23	78
9-10	M-635	20	4	14	3.2	28	93

Table 1: Recommended construction of $LCM_{1/2}$ from Figure B on page 3, as a function of the number of units in parallel. Uses PTFE stranded wire conforming to MIL-W-16878/4.

Power Ratings

Continuous Power Rating

Steady-state output power is rated to 1500 W for input line voltages above 100 Vrms (L-N). This rating is based on a +MIDBUS current of 7.5 A, providing design margin against the (minimum) 9.5 A current limit specification. For a +MIDBUS voltage of 200 V, 7.5 A equates to 1500 W. As the steady-state +MIDBUS voltage is reduced for input line voltages below 100 Vrms, the power rating is also reduced proportionately: at 85 Vrms +MIDBUS is nominally 170 V and the corresponding power rating is 1275 W (see Figure 11).

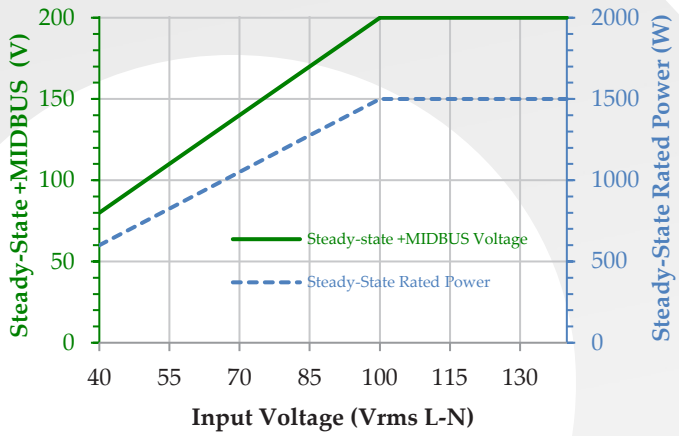


Figure 11: Steady-state +MIDBUS voltage and rated output power vs. AC line voltage. Unit will run down to UVLO at 40 Vrms (L-N), but AC GOOD will be pulled low below 80 Vrms (L-N). AC GOOD must be valid to allow initial startup.

Thermal Management

Advanced thermal management techniques are employed to create a very low thermal resistance from power devices to baseplate, while retaining SynQor's standard SMT construction and mechanically compliant potting compound. At 1.5 kW load, internal power devices run at about 20 °C above the baseplate temperature. This makes full rated power available even at a baseplate temperature of 100 °C (see Figure 12).

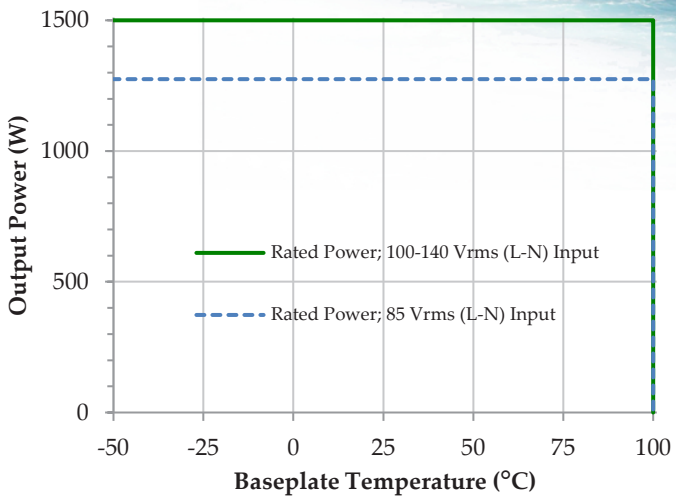


Figure 12: Rated steady state power vs. baseplate temperature. See Figure 11 for rated power vs. line voltage.

+MIDBUS Current Limit

The buck stage contains an output current limit at 10 A +/- 5%. Because the +MIDBUS voltage is reduced at low input voltage, the maximum available power is reduced at low line (see Figure 11). Thermally, the unit can operate indefinitely near this current limit while maintaining internal temperatures to less than 125 °C, provided the baseplate is maintained at or below 85 °C.

Since +VOUT is regulated, the input to the boost stage is constant-power: if +MIDBUS falls, the boost input current will rise. Therefore, if the unit is loaded from +VOUT such that the buck 10 A current limit becomes activated, the +MIDBUS voltage will collapse at a rate governed by the capacitance at +MIDBUS. It is therefore recommended to operate the converter at or below rated power in steady state, approaching current limit only during transient events.

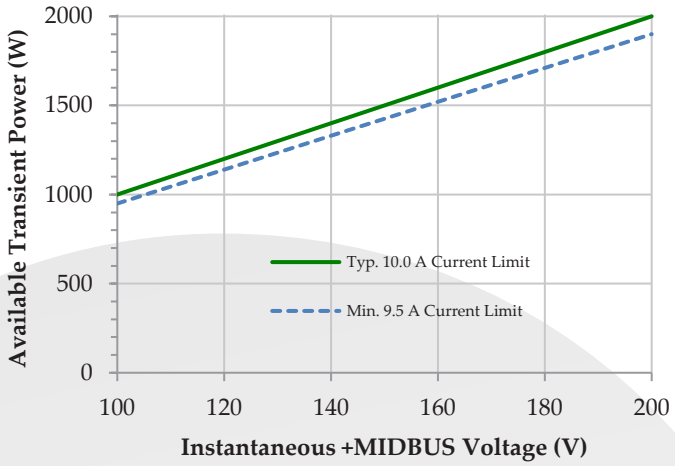


Figure 13: Available transient power vs. instantaneous +MIDBUS voltage. See Figure 11 for steady-state voltage.

The current limit is linearly controlled and has no fold-back. Under many conditions, the unit can hit current limit during a transient and recover without shutting down. To determine whether the unit will run through a line or load transient:

1) First determine the minimum +MIDBUS voltage encountered during the transient, which will generally be lower than the steady-state value shown in Figure 11. The minimum +MIDBUS voltage value is a function of the transient severity and the value of +MIDBUS capacitance: this is graphed in Figure 14 for load transients, but must be measured for line transients.
2) Multiply this minimum +MIDBUS voltage by 9.5 A (the worst-case minimum value for +MIDBUS current limit) to obtain the minimum value during the transient for available power (see Figure 13).
3) If this minimum available power is greater than the load power applied during the transient, then the unit will recover after the transient. If the load power is higher than available power during the transient, then +MIDBUS will collapse. The unit will turn off whenever +MIDBUS is below 50 V for more than 150 ms and will auto restart after 1 second.

Load Transients

Transients applied at either +VOUT or +MIDBUS will cause a significant dip in voltage at +MIDBUS, which must remain high enough to sustain the applied load power, as shown in Figure 13. Higher values of external capacitance at +MIDBUS will reduce the deviation seen during a load transient, as shown in Figure 14.

For instance, with 100 µF of external +MIDBUS capacitance, a transient from 0% to 75% rated power is handled easily: as seen in Figure 13, the required +MIDBUS voltage to sustain 75% power is only 120 V. However, a full 0% to 100% load transient requires at least 160 µF of external capacitance to keep +MIDBUS from dipping below the required 160 V and then collapsing. See section above entitled "+MIDBUS Current Limit" for more information.

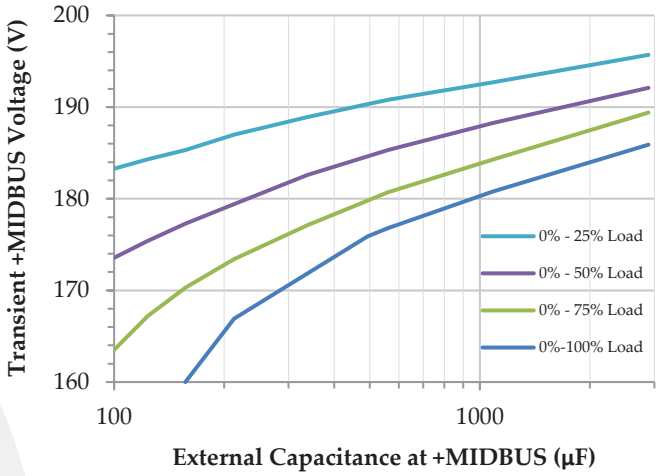


Figure 14: Instantaneous minimum value of +MIDBUS voltage during a (constant-current) load transient vs. external capacitance placed at +MIDBUS, shown at various load step amplitudes.

Power Interrupts and Holdup

Many systems need to operate through brief interruptions of AC input power. External capacitors placed at +MIDBUS, +VOUT, or both can be used to maintain power flow to critical loads during these input power interruptions.

Holdup Capacitor Position

When the bulk holdup capacitor is located at +MIDBUS, the capacitor voltage can dip during a line dropout while +VOUT remains relatively undisturbed. The boost stage is able to maintain its normal output down to a +MIDBUS voltage of 135 V. The voltage rating for capacitors at +MIDBUS should be at least 240 Vdc.

Holdup capacitance may instead be placed at +VOUT if dips in the output voltage are acceptable during a line interruption. During a line brownout, the diodes in the buck PFC stage remain reverse-biased until the +MIDBUS voltage drops below the level shown in Figure 11. Using relatively low capacitance at +MIDBUS allows the +MIDBUS voltage to drop to this level quickly, allowing the converter to contribute some power to +VOUT (see Figure 13). The voltage rating for capacitors at +VOUT should be at least 320 Vdc.

The internal PFC bias supply can be powered either from the line or from +VOUT. If a line interruption occurs, the unit will

stay alive provided +VOUT stays above 115 Vdc. The boost stage includes a bypass diode so that +VOUT is never more than a diode drop below +MIDBUS.

Holdup Capacitor Value

The holdup capacitor must store a certain amount of energy:

$$E_{holdup} = P_{out} \cdot t_{drop}$$

where:

P_{out} is the output power during the holdup event

t_{drop} is the duration of the input power interruption

Based on this energy requirement, the holdup capacitor value is:

$$C_{holdup} > \frac{2 \cdot E_{holdup}}{(V_i^2 - V_f^2)}$$

where:

V_i is the initial holdup capacitor voltage immediately before the input power interruption.

V_f is the minimum capacitor voltage during the transient. (For cap at +MIDBUS, determine from Figure 13; for cap at +VOUT, determine based on downstream requirements.)

The above equation is graphed in Figure 15 for holdup capacitance at +MIDBUS and Figure 16 for holdup capacitance at +VOUT.

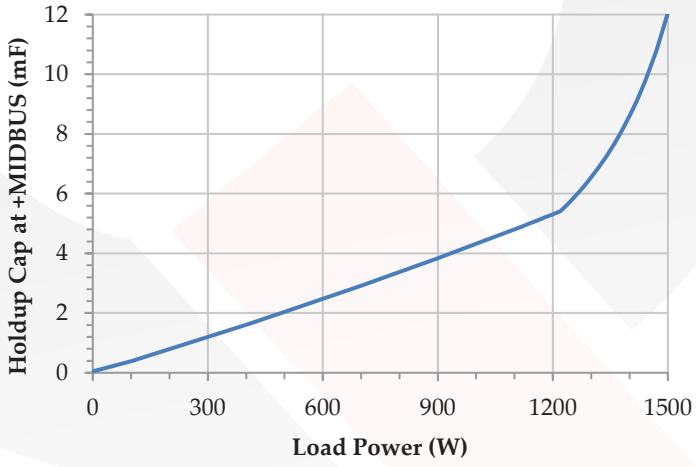


Figure 15: Minimum holdup capacitance required at +MIDBUS to ride through a 50 ms line interruption, keeping +VOUT in regulation as seen in Figure 17. Capacitor must be rated to ≥ 240 V.

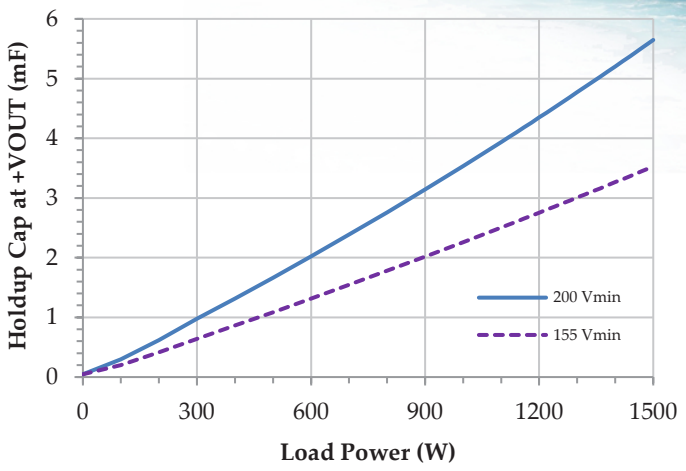


Figure 16: Minimum holdup capacitance required at +VOUT to ride through a 50 ms line interruption, allowing +VOUT to drop to 200 V or 155 V. Capacitor must be rated to ≥ 320 V

When the holdup capacitor is located at +MIDBUS, V_i will be a function of line voltage (see Figure 11) and load current (+MIDBUS will typically droop to 200 V at full load). V_f will be a function of load power during line interruption because of the +MIDBUS current limit (see Figure 13 and further discussion in the section entitled "+MIDBUS Current Limit").

Bulk holdup capacitance may also be placed at +VOUT if the system can tolerate a large voltage dip during line interruption. For instance, SynQor MCOTS-C-270 series converters have a continuous input rating down to 155 V. Two-thirds of the available energy can be extracted from the +VOUT capacitor as it discharges from 270 V, reducing the necessary capacitor physical volume.

SynQor MCOTS-B-270 series isolated bus converters have tremendous power density, but with their fixed-ratio conversion, dips at the input are reflected directly to dips at the output. It may be desired to achieve the +VOUT response shown in Figure 17 by locating bulk capacitance at +MIDBUS.

A significant safety margin on the holdup capacitor value is recommended to account for the following cumulative effects:

1) Capacitor tolerance, aging, and temperature variation
2) Capacitor ESR and diode losses during the interruption
3) Variation in the initial voltage V_i due to line & load conditions immediately preceding the input power interruption
4) Current limit tolerance (9.5 A minimum, which raises the required V_f to sustain load power as shown in Figure 13)
5) Boost stage efficiency (see Figure 2: 98.5% at full load)
6) Fall and rise time of the input voltage, which increase the interval over which the PFC is unable to deliver power into +MIDBUS

Figure 17 shows an example of a 50 ms line interruption. Note that for the conditions in Figure 17, the ideal equation would predict C_{holdup} > 6 mF. Yet the actual capacitor used was 7.5 mF, chosen to keep the minimum voltage well above the available transient power shown in Figure 13 and to account for the combined effects of items 1, 2, 5, and 6 discussed above.

When full load is drawn during a long input power interruption, the holdup capacitor physical size quickly becomes unreasonable. Furthermore, repetitive transients require surplus energy during the recovery time. It is possible to reduce holdup power significantly by disabling non-critical loads when the AC GOOD signal goes low.

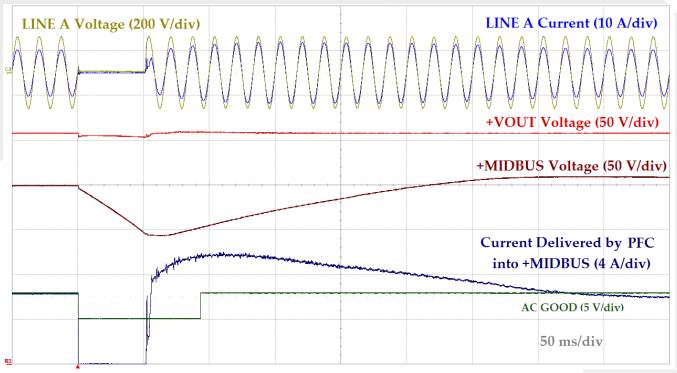


Figure 17: Response to 50 ms line interruption; 60 Hz; 1250 W power drawn from +VOUT pin; 7.5 mF total capacitance placed at +MIDBUS with series R || D network as shown in Figure 18.

Holdup during AC Line Brownout

When considering recovery from a line dip / brownout, t_{drop} from the above C_{holdup} equation must be carefully defined as the time during which the PFC is unable to recharge +MIDBUS. The PFC will be unable to contribute any power when +MIDBUS is above the nominal value shown in Figure 11 because diodes in the buck topology PFC stage become reversed biased and no current will flow. Therefore, during a line brownout, the +MIDBUS capacitor will need to supply the whole load demand until the +MIDBUS voltage discharges below the line shown in Figure 11 after which the buck PFC can supply up to 10 A (typ.) / 9.5 A (min.) into +MIDBUS.

It is possible to run through extended brownouts provided that the power demand from +MIDBUS stays below the available power shown in Figure 11. If the power exceeds this level, then the excess power must come from the +MIDBUS capacitor, and +MIDBUS voltage will collapse at a rate proportional to the excess power (and inversely proportional to the +MIDBUS capacitance). The unit will run indefinitely down to 40 Vrms (the input UVLO threshold) at reduced power, even after the AC GOOD signal is pulled low below 80 Vrms. Likewise, the unit will run indefinitely during voltage surges above 140 Vrms. Line voltage must be within the AC GOOD thresholds for initial startup.

Holdup during AC Line Surges

Large AC line transients can, in some cases, trip either "Short Circuit Current Limit" or "Input Over-Voltage Protection." In response, the unit will interrupt power flow for 240 µs or 1 ms, respectively. This should be treated as a line interruption; significant external holdup capacitance will typically be required to keep the output in regulation through this type of transient. See the section above entitled "Holdup Capacitor Value" for further analysis.

R||D Network for Large Holdup Capacitors

Capacitance in excess of the 1 mF maximum value requires an additional series R||D network for optimum stability, as shown in Figure 18. The diode must be rated for at least 300 V and a fast recovery type is recommended to improve forward recovery characteristics. The resistor must be adequately rated for pulse capability: a ceramic composition type is recommended. See Figure B on page 3 for suggested resistor and diode part numbers.

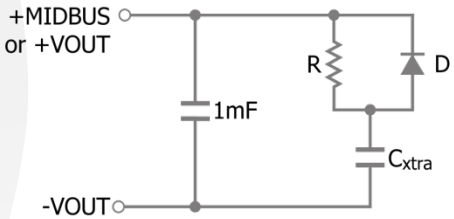


Figure 18: Series R||D network for capacitance at +MIDBUS or +VOUT in excess of 1 mF

For capacitors between 1 mF and 10 mF, the resistor value shown in Figure 18 should be 4.7 Ω. Capacitors larger than 10 mF may be used, but it is possible to trip the "+MIDBUS Under-Voltage Shutdown" protection if +MIDBUS does not reach 50 V within 150 ms after it begins to ramp up. Increasing the resistor value to 10 Ω will circumvent this protection feature by causing the +MIDBUS voltage to quickly rise above 50 V due to the voltage drop across the resistor while in current limit. However, a 10 Ω value also increases the capacitor recharge time, affecting the ability to run through repetitive transients.

PULSED LOADS

Pulsed Loads and Input Harmonics

The CE101 input harmonics shown in Figure 19 were measured with a DC load. If instead, the system under test involved a pulsed load, the pulsed power could be reflected back to the input and might cause a compliance failure.

Special constant-power control in the PFC is able to help significantly.

Conditions for Constant Input Power Control

The 3-phase PFC has two modes of control. Within +/- 10 V of the nominal +MIDBUS set point, the buck stage output approximates a constant-power characteristic. If the +MIDBUS capacitance is adequately sized, this special control forces the capacitor to absorb (and deliver) a large fraction of the load pulse energy, and thus helps prevent the load variation from appearing on the AC input lines. Within the +/- 10 V constant power window, average power flow is adjusted slowly, with a 40 ms time constant.

If on the other hand, the pulsed load is too large or +MIDBUS capacitance is too small, and +MIDBUS deviates from nominal by more than +/- 10 V, then the controller will switch modes and attempt to quickly regulate the +MIDBUS voltage. This necessarily draws transient currents from the AC input.

By way of example, consider a 500 W load that pulses to 1.5 kW for 2 ms, repeating every 10 ms. This load can be considered a constant 700 W superimposed with a 100 Hz repetitive transient (+800 W @ 20% duty & -200 W @ 80% duty). If the +MIDBUS capacitor can supply the full transient energy (800 W for 2 ms = 1.6 J) while slewing +MIDBUS by less than 20 V, the PFC input will draw essentially constant input power. Capacitor energy supplied during the transient is $\Delta E = C \cdot V \cdot \Delta V$ *or* $C = \Delta E/(V \cdot \Delta V)$. In this example, $C = 1.6\,J/(200\,V \cdot 20\,V) = 400\,uF$; when $C_{MB} > 400\,uF$, the unit will operate with constant input power.

A general solution for the minimum +MIDBUS capacitance necessary to enable constant power control may be expressed as:

$$C_{MB} > \frac{(P_{max} - P_{av}) \cdot D_{max}}{f_{tran}} \cdot \frac{1}{V_{MB} \cdot \Delta V_{MB}}$$

or

$$C_{MB} > \frac{(P_{av} - P_{min}) \cdot D_{min}}{f_{tran}} \cdot \frac{1}{V_{MB} \cdot \Delta V_{MB}}$$

where values in parenthesis are from the above example:

P_{av} is the pulsed load average power (ex. 700 W)

P_{max} is the pulsed load maximum power (1500 W)

P_{min} is the pulsed load minimum power (500 W)

D_{max} is the maximum power duty cycle (0.2)

D_{min} is the minimum power duty cycle (0.8)

f_{tran} is the pulsed load frequency (100 Hz)

V_{MB} is 200 V, the nominal +MIDBUS voltage.

ΔV_{MB} is 12 V, applying a safety factor to the 20 Vpk-pk maximum +MIDBUS voltage deviation required to maintain constant power control.

The +MIDBUS capacitor does not necessarily need to be large enough to satisfy the above equation. In applications where the load transients are small, or where AC input current transients are acceptable, less capacitance may be used at +MIDBUS.

+VOUT Capacitance

Additional capacitance at +VOUT is required for applications with pulsed loads applied at +VOUT where the peak power is above 2 kW. In this case, the capacitance should be increased until the +VOUT capacitor sources enough of the load pulses to reduce the peak boost power below 2 kW. This prevents activation of the cycle-by-cycle boost current limit.

The minimum recommended capacitance at +VOUT varies linearly with the maximum load current. If the highest expected load current is half the rated value, then the capacitance at +VOUT may also be reduced by half. If the system draws power exclusively from +MIDBUS, then no external capacitance is required at +VOUT.

Downstream power converters will have separate requirements for stabilizing capacitance. Input system instability is possible at the input of any regulated power converter (see "Input System Instability" whitepaper). If input power of this downstream converter is constant, then an incremental decrease in voltage will cause the converter to draw more current. This can be modeled as a negative resistance (valid at frequencies DC up to the converter input-voltage feed-forward control bandwidth). Combined with an inductive source, this negative resistance can cause large oscillations, which are most likely to occur at the lowest source voltage and highest operating power. The typical solution is to add a known positive resistance in series with a sufficiently large capacitor across the input of any downstream power converter. Since stability will depend on both the design of the downstream converter and the selected external capacitor value / series resistance, it is best to verify downstream converter stability in the final application.

External Capacitor Selection

Capacitors connected externally at +MIDBUS should have a rating of 240 V or higher. For +VOUT, the rating should be at least 320 V. Standard aluminum electrolytic capacitors are acceptable but have several significant drawbacks:

1) Narrow temperature ratings
2) Relatively high ESR at room temperature
3) Very high ESR at low temperature
4) Poor reliability at high temperature

Conductive polymer solid electrolytic capacitors solve all four of these problems at the expense of somewhat lower energy density:

1) Rated for full -55 °C to 125 °C temperature range
2) Good ESR at room temperature

3) Rated to maintain good ESR at low temperature
4) Much better reliability

These solid electrolyte capacitors are currently only widely available with continuous DC voltage ratings of 80 V and below (for example, Nichicon series PCR). The available evaluation board schematic shows these capacitors connected in series for higher total ratings with a simple discrete circuit to keep individual capacitor voltages balanced.

PROTECTION FEATURES

Over-Temperature Shutdown

An integrated temperature sensor protects the unit from accidental damage by disabling the unit when internal sensor temperature rises above 125 °C. At full rated power, this corresponds to a baseplate temperature of 110 °C (higher at reduced loads). The unit automatically restarts after the internal sensor cools below 120 °C.

Over-temperature shutdown can be disabled (along with phase drop shutdown) by connecting the $\overline{\text{BATTLE SHORT}}$ signal to CTL RETURN. When not externally driven low, a high state on the $\overline{\text{BATTLE SHORT}}$ pin indicates that either over-temperature or phase-drop shutdown is imminent. The over-temperature warning threshold is 120 °C (measured at the internal sensor), corresponding at full load to a baseplate temperature of approximately 105 °C (higher at reduced loads).

With the main over-temperature shutdown disabled, a redundant protection remains in place which will turn off both the unit and the 3.3V AUX supply when the bias supply IC temperature goes above approximately 160 °C. At full load, this corresponds to a baseplate temperature of approximately 145 °C (higher at reduced loads).

Phase Drop Shutdown

In the event of a loss of one line phase, the unit will shut down after a delay of 0.25 seconds, and will automatically restart approximately 1 second after normal three-phase power is restored. During the phase drop, the unit will attempt to deliver power from the remaining two input line phases. However, phase-drop (and over-temperature) shutdown can be disabled by externally connecting the $\overline{\text{BATTLE SHORT}}$ signal to CTL RETURN in which case the unit will attempt to deliver power throughout a phase-drop event. When not externally driven low, a high state on the $\overline{\text{BATTLE SHORT}}$ pin indicates that either phase-drop or over-temperature shutdown is imminent.

Short Circuit Current Limit

In most overload conditions, the linear 10 A buck current limit is sufficient. A backup "short-circuit current limit" circuit handles severe input transients or output short-circuit events. Redundant current sense resistors and comparators are connected in series with both the positive and negative sides of the buck PFC stage, set to trip well above the linear current limit threshold. When this backup protection is activated, the unit will respond by turning off all power flow from the input for approximately 200 µs, after which normal operation resumes immediately.

Input Over-Voltage Protection

If the instantaneous voltage between any two line inputs goes above the threshold of 500 V (L-L), then all power flow from the input will be interrupted, resuming 1 ms after the input voltage falls again below the same threshold. (Voltage spikes shorter than 80 µs may not trigger this protection response.) During an interruption, the +MIDBUS voltage will fall at a rate determined by capacitance and load current. The amount capacitance needed to maintain normal operation during this 1 ms interruption may be calculated as shown in the section entitled "Holdup Capacitor Value."

Input Under-Voltage Shutdown

The input voltage must be above 81 Vrms (L-N) to activate AC GOOD and allow the unit to start up. If the input voltage subsequently drops below 40 Vrms (L-N) for more than 1 second the unit will shut down. The unit will stay off for at least 1 second.

Boost Current Limit

An independent current sense resistor and comparator implement a hardware cycle-by-cycle current limit in the boost stage, set to a boost input current of approximately 14 A. The boost stage is in series with the buck stage, and the buck current limit is set to 10 A, so the boost current limit is only active in abnormal situations. A bypass diode is connected internally between +MIDBUS and +VOUT to provide further short-circuit protection.

Output Over-Voltage Protection

A redundant hardware over-voltage protection circuit will disable the boost stage on a cycle-by-cycle basis if +VOUT ever rises above 310 V. The unit resumes normal operation immediately after the output voltage returns below this threshold.

+MIDBUS Under-Voltage Shutdown

Should the action of the linear 10 A buck current limit reduce the +MIDBUS voltage to less than 50 V for more than 150 ms, the unit will assume a sustained overload and will shut down. Auto-restart will occur after 1 second. This feature is also present during startup and thus serves to limit energy delivered into a shorted output.

Pre-bias / Reverse Power Flow

Both the buck and boost stages have diode rectification that prevents reverse power flow whether the unit is enabled or disabled. It is acceptable to start up with voltage present and/or to connect external voltage sources to +MIDBUS / +VOUT. If a downstream power converter experiences reverse power flow, the PFC module will be unable to avoid an output over-voltage condition because it cannot sink current.

EMI Recommendations

Input Filtering

As shown in figure A, it is recommended (although not required) to pair the PFC module with the separately available MACF-115-3PH-UNV-HT half brick 3-phase AC input filter module. The available evaluation board using this external filter with the PFC module was demonstrated to pass the CE101 and CE102 requirements as part of MIL-STD-461 testing at an independent laboratory (see "CE101 and CE102 Measurements" below). For this testing, the evaluation board was mounted in a box along with a 1.5 kW resistive load and cooling fans.

Without an input filter, the full load input noise level (as measured by a standard 50 µH LISN) is 0.28 Vrms (109 dBuV) at the main switching frequency. With the specified input filter, this is reduced by approximately 45 dB to 1.6 mVrms (64 dBuV). Since noise levels are very small, care must be taken to minimize external coupling to the unshielded input lines between the filter and LISN.

If further noise reduction is desired at the main switching frequency near 200 kHz, additional differential-mode inductance may be added in series with each of three line inputs, placed between the external filter module and PFC module. Likewise, it is acceptable to have a relatively long cable run between the filter and PFC module. Surge protection devices should be located directly at the PFC module input.

CE101 and CE102 Measurements

Conducted emissions were measured by an independent laboratory. Standard 50 µH LISNs were used with an input line frequency of 400 Hz. Results are shown below for power levels of 1500 W, 1000 W, and 500 W. Per spec, the limit line in each CE101 graph is set relative to the amplitude of input current at the 400 Hz fundamental (the highest peak in each CE101 chart below). All EMI testing used the SynQor 3-phase AC input line filter, part number MACF-115-3PH-UNV-HT mounted on the standard evaluation board.

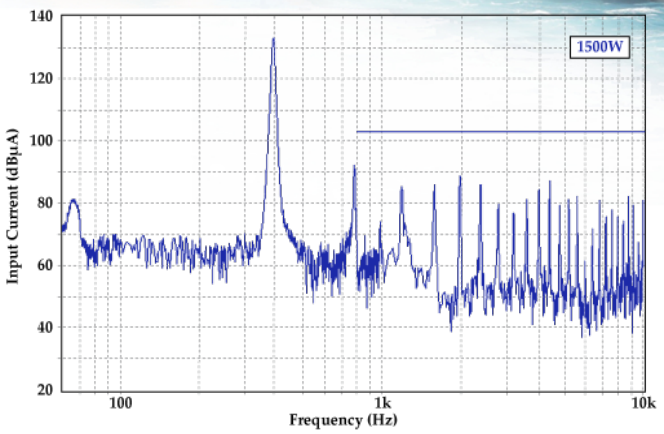


Figure 19: CE101 data at 400 Hz and 1500 W output power.

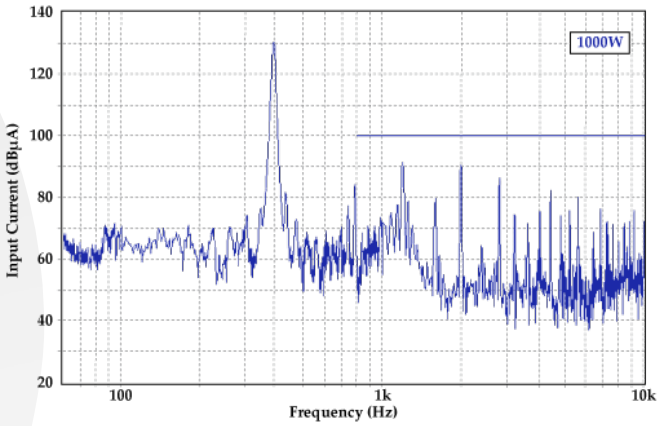


Figure 20: CE101 data at 400 Hz and 1000 W output power.

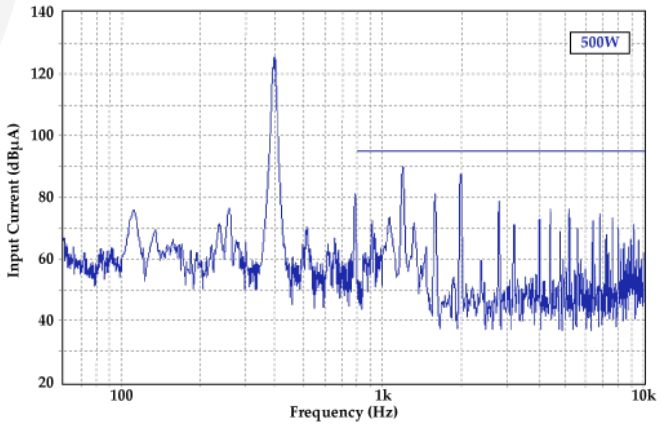


Figure 21: CE101 data at 400 Hz and 500 W output power.

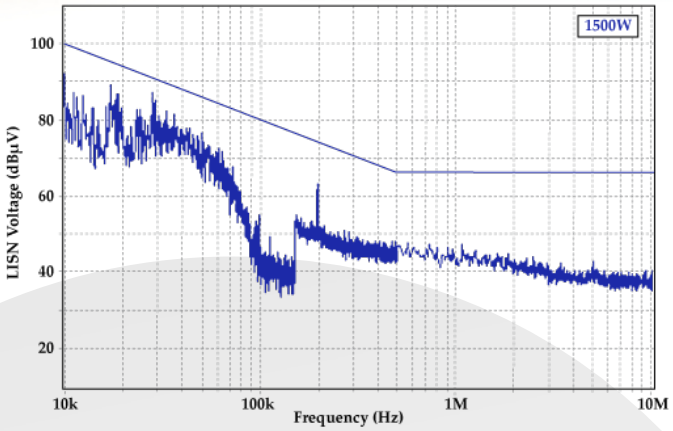


Figure 22: CE102 data at 400 Hz and 1500 W output power.

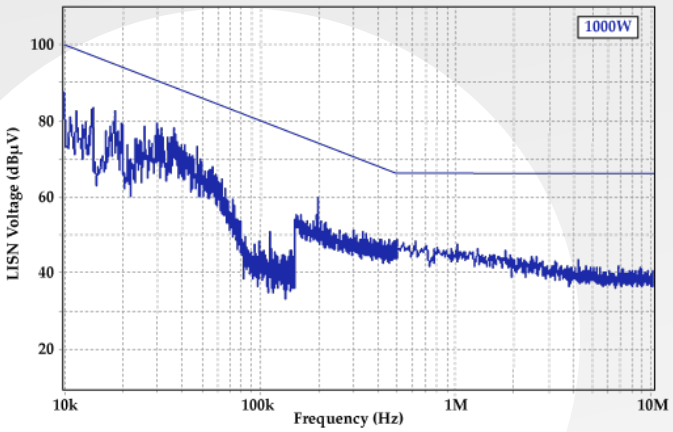


Figure 23: CE102 data at 400 Hz and 1000 W output power.

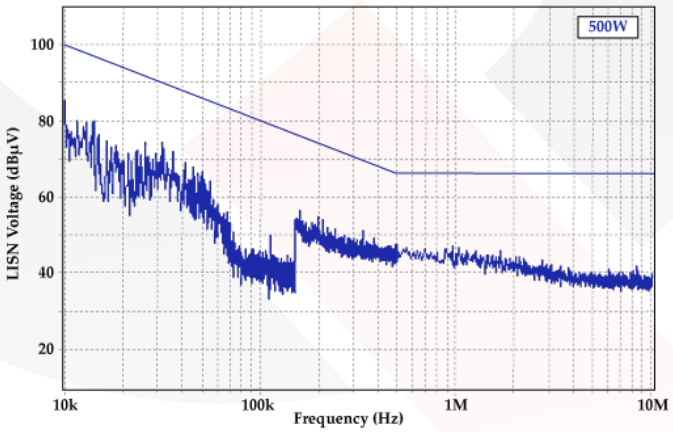


Figure 24: CE102 data at 400 Hz and 500 W output power.

Input Protection

The input stage implemented in this module offers far better immunity from input surges than a traditional boost topology. In a traditional boost PFC, there is no mechanism to limit current flow directly from input to output during operation, so for long duration surges, the current becomes very large and results in permanent destruction. In contrast, the buck PFC input stage used in this module is able to interrupt current flow during a voltage surge which dramatically lowers device stresses.

The PFC input lines must be protected from spikes which might exceed their 575 Vpk (L-L) absolute-maximum rating. It is recommended to add external protection devices directly between the three pairs of PFC line input pins. Figure A shows an example input protection circuit consisting of clamping devices connected line-line in a "delta" configuration, one set before and one set after the external MACF-115-3PH-UNV-HT input filter module. The set of Metal Oxide Varistors (MOVs) upstream of the filter prevent local arcing during a surge event due to input wiring inductance. These MOVs have a "soft" breakdown characteristic: at high currents they will clamp at a relatively high voltage. The set of special TVS devices downstream of the filter module have far superior characteristics. These AK3-430C devices made by Littelfuse (or equivalent Bourns PTVS-430C-TH) have superb clamping voltage: even at high currents they hold the input voltage below the 575 Vpk (L-L) absolute maximum specification of the PFC module. In order to prevent damage in the MPFC from surges or spike, the input voltage to the module must be clamped by TVS devices. The AK3 devices also have high energy capability: whereas standard TVS devices have a relatively small die, the AK3 series parts have many large dies stacked on top of each other. This allows the AK3 to withstand very high energy repetitive transients while the voltage across the module's input pins remains safely clamped. Protection devices in the end user application should be tailored to the expected surge requirements and the MPFC maximum voltage rating. Fuses rated for 10 A are recommended in series with each input line, located upstream of the MOVs.

Baseplate Electrical Connection

All circuitry in the PFC module is electrically isolated from the baseplate with a multi-layer solid insulator. This isolation barrier meets basic insulation requirements and is 100% hi-pot tested in production to 2150 Vdc. The baseplate and corner mounting posts may therefore be connected to protective earth ground in the application circuit. Maintain adequate clearance from all external circuitry to the four corner mounting posts, which are electrically connected to the baseplate.

SHIELD (Pin 8)

The SHIELD net is internally coupled via capacitors to both the input and output voltages and is therefore able to locally contain high frequency electromagnetic emissions. If desired, this pin may be connected to a floating shield plane underneath the unit, but must always be left floating. When the unit is soldered into a PCB, this lower SHIELD plane would typically be constructed on one of the top-most PCB

layers. Internal bleeder resistors maintain the SHIELD pin at the pseudo-neutral line potential. The SHIELD net is also internally connected to an integral upper copper plane between the power switching devices and the baseplate.

Control Pins

START SYNC (Pin A1)

Pin A1 is designated as START SYNC, and is only implemented on the *270P* option (i.e. MPFC-115-3PH-270P-FP…). This pin is not used on the standard model (i.e. MPFC-115-3PH-270-FP) and should be left floating when not used. In paralleled applications, connect START SYNC between multiple units to synchronize restart after a fault condition. See section entitled "Features of *270P* Option" for further details. Internal interface circuitry is shown in Figure 29.

CTL RETURN (Pin A2)

CTL RETURN serves as the ground reference for all control signals. 1 kV of functional isolation is provided between all control pins and the power pins. CTL RETURN may be externally connected to any of the power pins, attached to an application circuit, or left floating. Safety isolation is not provided, so connecting CTL RETURN to the output of downstream isolated DC/DC converters would defeat any safety rating provided by these converters. If required, external safety-rated isolators could be powered from 3.3V AUX.

SERIAL IN (Pin A3)

A wide variety of operating parameters (voltages, currents, temperatures) may be accessed via the built-in full-duplex asynchronous serial interface. With the *270P* option, it is also possible control the $\overline{\text{BATTLE SHORT}}$ and $\overline{\text{PFC ENA}}$ pin functions via the serial interface. Commands may be transferred to the internal DSP via the SERIAL IN pin at 9600 baud (8N1 – 8 data bits, no parity, 1 stop bit). A `start' or `zero' bit is encoded as a logic low. The internal baud rate will be exactly 20.48 times slower than the SYNC OUT frequency. The tolerance of both frequencies is better than +/- 2%. The frequency tolerance of the external interface circuit should also be better than +/- 2% accuracy to ensure that the last bit of incoming serial data arrives within the proper frame time. Alternatively, the SYNC OUT signal may be used to continuously calibrate the baud rate of the external interface circuit, allowing the use of a less accurate oscillator.

The SERIAL IN pin may be left open if unused, and will be internally pulled up to 3.3V AUX, corresponding to the `idle' or `stop' state. Internal circuitry is shown in Figure 25. Direct connection may be made to an external microcontroller, but an external transceiver IC is required to shift levels and polarity to drive from a standard RS-232 port (see evaluation board schematic). Safety isolation may be achieved using just one external digital isolator channel since there is no clock signal and the input/output direction is well defined. See the separate "MPFC-115-3PH-270-FP Serial Interface" companion document for detailed command syntax (available at www.synqor.com/pdf/MPFC-115-3PH-270-FP_Serial_Interface.pdf).

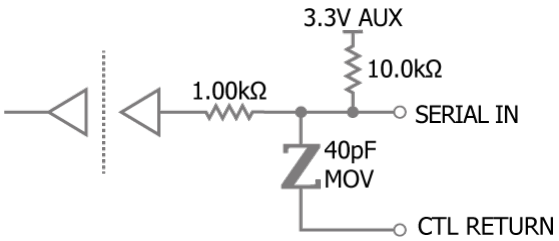


Figure 25: Internal circuitry for SERIAL IN pin.

SERIAL OUT (Pin A4)

A response to each command is sent via the SERIAL OUT pin at 9600 baud (8N1 – 8 data bits, no parity, 1 stop bit). The output is low for a `start' or `zero' bit. When not transmitting, the output is high, corresponding to the `idle' or `stop' state. Internal circuitry is shown in Figure 30. Direct connection may be made to an external microcontroller, but an external transceiver IC is required to shift levels and polarity to drive a standard RS-232 port (see evaluation board schematic). See the separate "MPFC-115-3PH-270-FP Serial Interface" companion document for detailed response syntax (available at www.synqor.com/pdf/MPFC-115-3PH-270-FP_Serial_Interface.pdf).

AC GOOD (Pin A5)

The unit will not turn on until the positive-logic AC GOOD output is high, typically for line inputs between 81 Vrms (L-N) and 149 Vrms (L-N). When the unit is already running, the AC GOOD output will typically transition low when the input voltage (at the PFC input pins) goes below 80 Vrms (L-N) or above 150 Vrms (L-N). Instantaneous line-to-line voltage measurements are used, so these voltage thresholds will be affected by imbalance in line phase and/or amplitude.

AC GOOD also responds to input line frequency. If the input line frequency goes out of range, AC GOOD will transition low (see page 5 for AC GOOD levels and tolerances).

AC GOOD generally only serves as a power interruption warning: the unit will continue to run if AC GOOD transitions low, the only exception being a phase-drop condition. The phase-drop shutdown feature will disable the unit 0.25 seconds after a power interruption unless this function is overridden by $\overline{\text{BATTLE SHORT}}$ (see "Phase Drop Shutdown" section).

The response time of AC GOOD to an input power interruption is less than 1 ms at 400 Hz and less than 5 ms at 60 Hz. AC GOOD will return to its normal high state 40 ms after the line voltage recovers. See Figure 17 for an example of

AC GOOD timing during a power interruption. Internal interface circuitry is shown in Figure 26.

DC GOOD (Pin A6)

During startup the positive-logic DC GOOD output will remain low until +VOUT crosses the 240 Vdc rising threshold (see Figure 27). The falling threshold at 140 Vdc is significantly lower, such that DC GOOD will usually remain high during an input power interruption. Therefore, DC GOOD is typically used to indicate successful startup, whereas AC GOOD is used to warn of an input power interruption. The typical DC GOOD response time is less than 1 ms. Internal interface circuitry is shown in Figure 26.

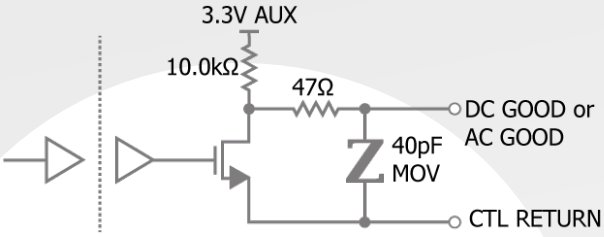


Figure 26: Internal circuitry for AC GOOD and DC GOOD pins.

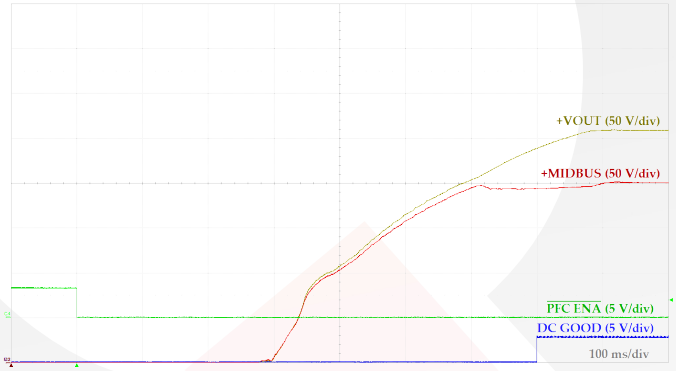


Figure 27: Timing from $\overline{\text{PFC ENA}}$ to startup and DC GOOD.

$\overline{\text{PFC ENA}}$ (Pin A7)

The $\overline{\text{PFC ENA}}$ pin must be brought low to enable the unit. A 10.0 kΩ pull-up resistor is connected internally to 3.3V AUX. Therefore, if all control pins are left floating, the unit will be disabled. The delay from enable to the beginning of the startup ramp is typically 300 ms (see Figure 27). Internal interface circuitry is shown in Figure 28.

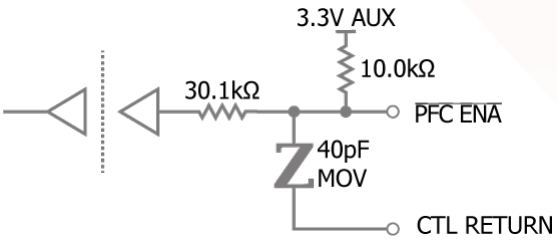


Figure 28: Internal circuitry for $\overline{\text{PFC ENA}}$ pin.

$\overline{\text{BATTLE SHORT}}$ (Pin A8)

If the $\overline{\text{BATTLE SHORT}}$ pin is externally pulled down to CTL RETURN, over-temperature protection and phase drop shutdown will be disabled. If the $\overline{\text{BATTLE SHORT}}$ pin is not externally held low, the pin will go high to warn of either an impending over-temperature shutdown or an input phase drop shutdown. The over-temperature warning engages 5 °C below shutdown. The input phase drop warning is engages 250 ms before shutdown. A 10.0 kΩ pull-up resistor is connected internally to 3.3V AUX. Internal interface circuitry is shown in Figure 29.

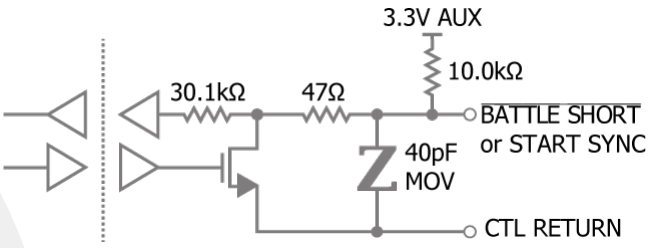


Figure 29: Internal circuitry for $\overline{\text{BATTLE SHORT}}$ and START SYNC pins.

3.3V AUX (Pin A9)

The 3.3V AUX supply is energized whenever AC power is present, regardless of the $\overline{\text{PFC ENA}}$ state, and is rated up to 100 mA at 3.3 V (relative to CTL RETURN). This independent supply is powered from either the line input or main output. If there is a line interruption but the +VOUT output voltage remains above 115 Vdc due to external holdup capacitance (at +VOUT or +MIDBUS), the 3.3V AUX output will remain live. 160 Vdc at the output is required to start the bias supply, a configuration sometimes used for serial port debugging without a full 3-phase AC source.

With the output disabled and with only 2 of 3 valid input line phases, there is adequate internal energy storage to keep the 3.3V AUX output in normal regulation if the line frequency is 400 Hz. With only 1 of 3 valid input line phases, the bias supply will typically shut down and periodically attempt to restart.

Some internal circuitry is also powered by 3.3V AUX, so if 3.3V AUX is externally shorted, the unit will be disabled.

SYNC OUT (Pin A10)

The SYNC OUT pin generates a continuous series of pulses at the main switching frequency. The duty cycle may (intentionally) vary between 5% and 50%, so only the rising edge should be used as a timing reference. The buck and boost converters are synchronized and switch at the same frequency. The SYNC OUT pin may be left open if not used. Internal interface circuitry is shown in Figure 30.

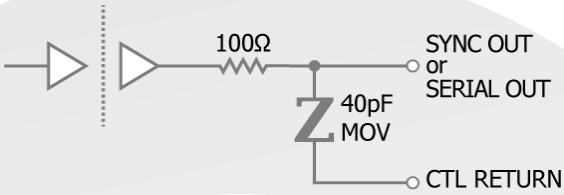
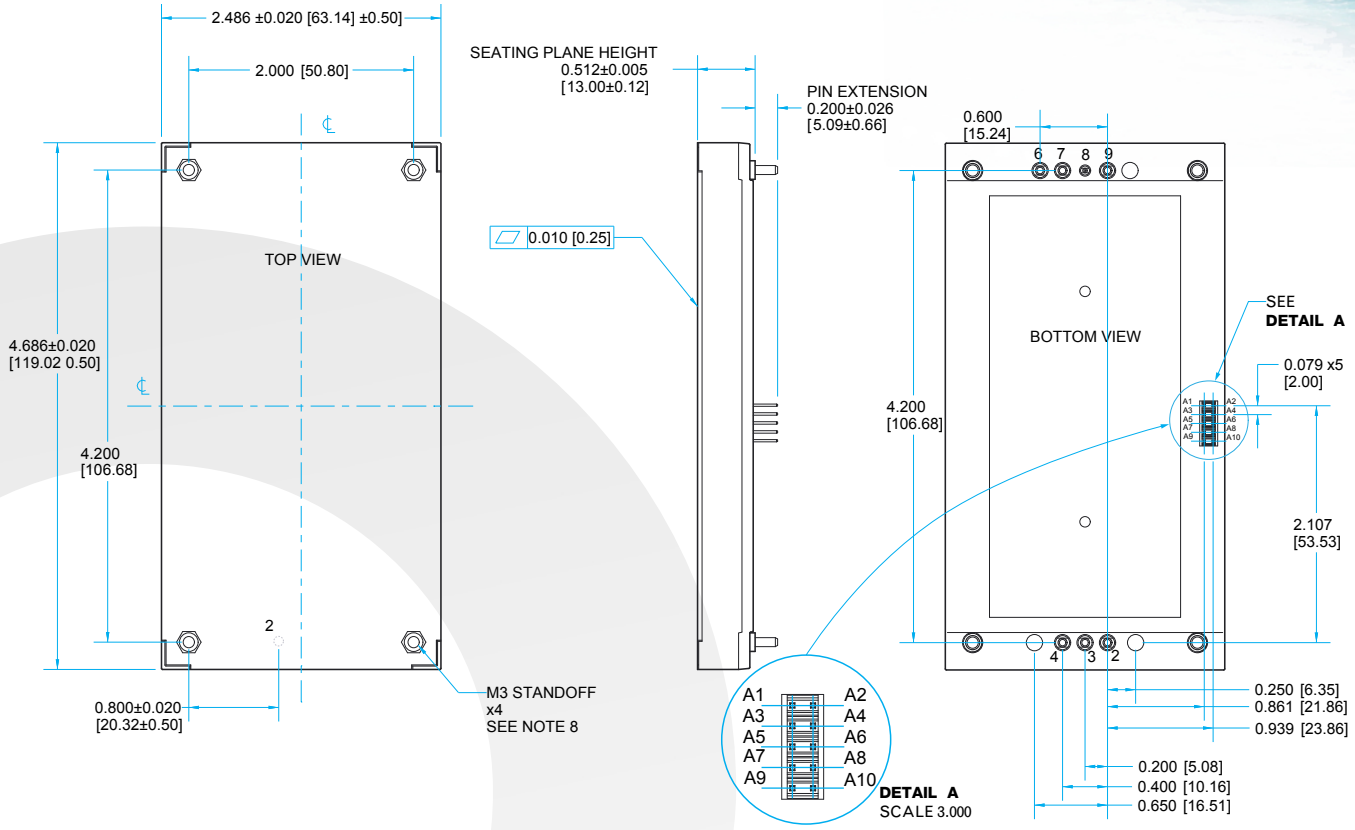


Figure 30: Internal circuitry for SYNC OUT and SERIAL OUT pins.

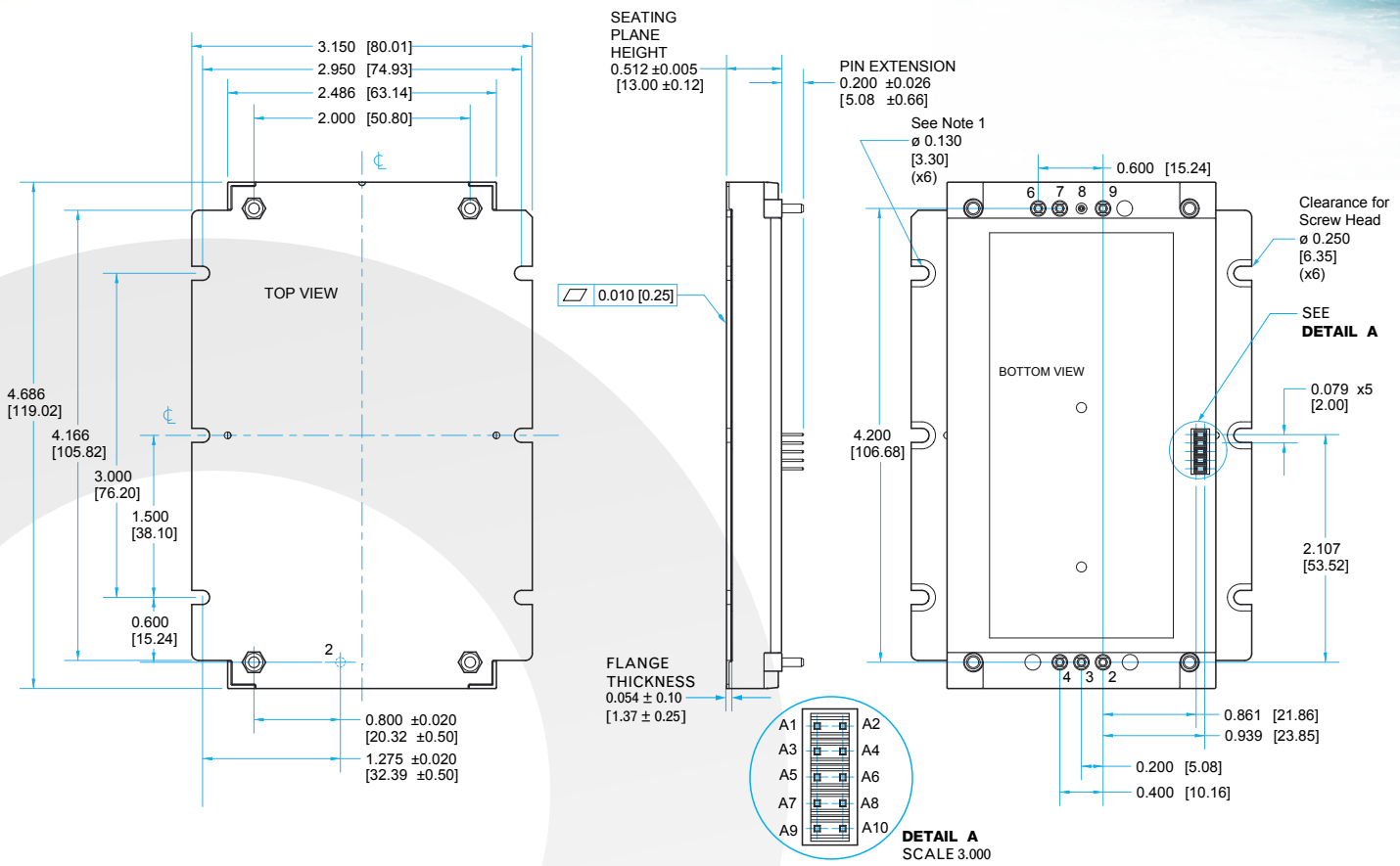


NOTES:

1. APPLIED TORQUE PER M3 SCREW SHOULD NOT EXCEED 6 in-lb (0.7 Nm)
2. BASEPLATE FLATNESS TOLERANCE IS 0.010" (0.25 mm) TIR FOR SURFACE.
3. PINS 2-4, 6, 7, AND 9 ARE 0.080" (2.03 mm) DIA. WITH 0.125" (3.18 mm) DIA. STANDOFF SHOULDERS
   MATERIAL: COPPER ALLOY. FINISH: MATTE TIN OVER NICKEL PLATE.
4. PIN 8 IS 0.040" (1.02 mm) DIA.
   MATERIAL: COPPER ALLOY. FINISH: MATTE TIN OVER NICKEL PLATE.
5. PINS A1-A10: 0.02" X 0.02" [0.51mm X 0.51mm]
   MATERIAL: PHOSPHOR BRONZE. FINISH: GOLD FLASH OVER NICKEL UNDERPLATING.
8. THREADED OR NON-THREADED OPTIONS AVAILABLE
9. UNDIMENSIONED COMPONENTS ONLY FOR VISUAL REFERENCE
10. ALL DIMENSIONS IN INCHES (mm)
    TOLERANCES: X.XX IN +/-0.020 (X.X mm +/-0.5 mm)
    X.XXX IN +/-0.010 (X.XX mm +/-0.25 mm)
11. WEIGHT: 11.3 oz (320 g)

PIN DESIGNATIONS

Pin	Label	Name	Function
2	LINE A	LINE A	AC Line A Input
3	LINE B	LINE B	AC Line B Input
4	LINE C	LINE C	AC Line C Input
6	+MIDBUS	+MIDBUS	Positive PFC Output / Boost Input Voltage
7	-VOUT	-VOUT	Negative Return for +VOUT and +MIDBUS
8	SHIELD	SHIELD	EMI Shield - Leave Floating
9	+VOUT	+VOUT	Positive Boost Output Voltage
A1	RESERVED	RESERVED	No Function (-270 Version)
	START SYNC	START SYNC	Startup Synchronization (-270P Version)
A2	CTL RETURN	CTL RETURN	Isolated Ground Reference for Pins A1 - A10
A3	SERIAL IN	SERIAL IN	Serial Data Input (High = Stop/Idle)
A4	SERIAL OUT	SERIAL OUT	Serial Data Output (High = Stop/Idle)
A5	AC GOOD	AC GOOD	AC Power Good Output (High = Good)
A6	DC GOOD	DC GOOD	DC Power Good Output (High = Good)
A7	PFC ENA	PFC ENA	Pull Low to Enable Unit
A8	BATTLE SHORT	BATTLE SHORT	Pull Low to Disable OTP / Phase Drop Shutdown
A9	3.3V AUX	3.3V AUX	3.3V @ 100mA Always-On Power Output
A10	SYNC OUT	SYNC OUT	Switching Frequency Synchronization Output



NOTES:

1. APPLIED TORQUE PER M3 OR 4-40 SCREW SHOULD NOT EXCEED 6 in-lb (0.7 Nm)
2. BASEPLATE FLATNESS TOLERANCE IS 0.010" (0.25 mm) TIR FOR SURFACE.
3. PINS 2-4, 6, 7, AND 9 ARE 0.080" (2.03 mm) DIA. WITH 0.125" (3.18 mm) DIA. STANDOFF SHOULDERS
   MATERIAL: COPPER ALLOY. FINISH: MATTE TIN OVER NICKEL PLATE.
4. PIN 8 IS 0.040" (1.02 mm) DIA.
   MATERIAL: COPPER ALLOY. FINISH: MATTE TIN OVER NICKEL PLATE.
5. PINS A1-A10: 0.02" X 0.02" [0.51mm X 0.51mm]
   MATERIAL: PHOSPHOR BRONZE. FINISH: GOLD FLASH OVER NICKEL UNDERPLATING
8. UNDIMENSIONED COMPONENTS ONLY FOR VISUAL REFERENCE
9. ALL DIMENSIONS IN INCHES (mm)
   TOLERANCES: X.XX IN +/-0.020 (X.X mm +/-0.5 mm)
   X.XXX IN +/-0.010 (X.XX mm +/-0.25 mm)
10. WEIGHT: 11.6 oz (326 g)

PIN DESIGNATIONS

Pin	Label	Name	Function
2	LINE A	LINE A	AC Line A Input
3	LINE B	LINE B	AC Line B Input
4	LINE C	LINE C	AC Line C Input
6	+MIDBUS	+MIDBUS	Positive PFC Output / Boost Input Voltage
7	-VOUT	-VOUT	Negative Return for +VOUT and +MIDBUS
8	SHIELD	SHIELD	EMI Shield - Leave Floating
9	+VOUT	+VOUT	Positive Boost Output Voltage
A1	RESERVED	RESERVED	No Function (-270 Version)
	START SYNC	START SYNC	Startup Synchronization (-270P Version)
A2	CTL RETURN	CTL RETURN	Isolated Ground Reference for Pins A1 - A10
A3	SERIAL IN	SERIAL IN	Serial Data Input (High = Stop/Idle)
A4	SERIAL OUT	SERIAL OUT	Serial Data Output (High = Stop/Idle)
A5	AC GOOD	AC GOOD	AC Power Good Output (High = Good)
A6	DC GOOD	DC GOOD	DC Power Good Output (High = Good)
A7	PFC ENA	PFC ENA	Pull Low to Enable Unit
A8	BATTLE SHORT	BATTLE SHORT	Pull Low to Disable OTP / Phase Drop Shutdown
A9	3.3V AUX	3.3V AUX	3.3V @ 100mA Always-On Power Output
A10	SYNC OUT	SYNC OUT	Switching Frequency Synchronization Output

Ordering Information

MPFC-115-3PH-270-FP
Input: 3Φ 115 Vrms (L-N)
Output: 270 Vdc
Power: 1.5 kW

Part Numbering Scheme						
Family	**Input Voltage**	**Output**	**Package Size**	**Thermal Design**	**Screening Level**	**Options**
MPFC	**115-3PH:** 3-Phase 115 Vrms L-N	**270:** 270 Vdc **270P:** 270 Vdc, Parallelable	**FP:** Full-brick Peta	**N:** Normal Threaded **D:** Non-Threaded **F:** Flanged Baseplate	**S:** S-Grade **M:** M-Grade	**[ ]:** Standard Feature

Example:MPFC-115-3PH-270-FP-N-M

PART NUMBERING SYSTEM

The part numbering system for SynQor's ac-dc converters follows the format shown in the example.

APPLICATION NOTES

A variety of application notes and technical white papers can be downloaded in PDF format from our website.

Contact SynQor for further information and to order:

Phone: 978-849-0600
Toll Free: 888-567-9596
Fax: 978-849-0602
E-mail: Power@synqor.com
Web: www.synqor.com
Address: 155 Swanson Road
Boxborough, MA 01719
USA

PATENTS

SynQor holds numerous U.S. patents, one or more of which apply to most of its power conversion products. Any that apply to the product(s) listed in this document are identified by markings on the product(s) or on internal components of the product(s) in accordance with U.S. patent laws. SynQor's patents include the following:

6,545,890 6,894,468 6,896,526 6,927,987 7,050,309 7,085,146
7,119,524 7,765,687 7,787,261 8,149,597 8,644,027

WARRANTY

SynQor offers a two (2) year limited warranty. Complete warranty information is listed on our website or is available upon request from SynQor.